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# 740 Family

Software Manual RENESAS MCU

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#### **REVISION HISTORY**

### 740 Family Software Manual

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		Page	Summary		
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		26	3.2 Instruction Set : Description revised.		
		31	ADC : Note 2 is revised.		
		53	CMP : Function revised.		
		60	DIV : Note 3 is added.		
		65	JMP : Note is added.		
		72, 133, 134	XX instruction cannot be used for any products $\rightarrow$ XX instruction cannot be used		
			for <u>some</u> products.		
		72	MUL : Note 3 is added.		
		74	ORA : N is when bit 7 $\rightarrow$ N is <u>"1"</u> when bit 7		
		78	PLP : Note is added.		
		82	RTI : Status flag is revised.		
		83	RTS : Operation is revised.		
		84	SBC : Note 2 is revised.		
		101	WIT : Function is revised.		
		102 to 104	3.4 Instructions Related to Interrupt Processing and Subroutine Processing added.		
		105	NOTES ON USE : "4.1 Notes on input and output ports" is added.		
		107	Fig. 4.3.1 is revised.		
			4.3.2 : Description revised.		
		108	4.3.3 Distinction of interrupt request bit : Description revised.		
			Fig. 4.3.2 is revised.		
		110	Fig. 4.4.4 is revised.		
		111	"4.4.5 Multiplication and division instruction", "4.4.6 Ports" and		
			"4.4.7 Instruction execution time" are added.		
		112	Valid signal for each product : Table is revised and note is added.		
		178	Part of instruction table is revised.		
		184	Part of instruction code is revised.		
			Table of products which unuse these instructions is eliminated.		
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# **Using This Manual**

This software manual is written for the 740 Family. It applies to all microcomputers integrating the 740 Family CPU core.

The reader of this manual is assumed to have a basic knowledge of electrical circuits, logic circuits, and microcomputers.

#### 740 Family Documents

The following documents were prepared for the 740 family.

Document	Contents
Data Sheet	Hardware overview and electrical characteristics Hardware specifications (pin assignments, memory maps, peripheral specifications, electrical characteristics, timing charts).
Software Manual	Detailed description of assembly instructions and microcomputer performance of each instruction
Application Note	<ul><li>Usage and application examples of peripheral functions</li><li>Sample programs</li></ul>

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#### **1. OVERVIEW**

The distinctive features of the CMOS 8-bit microcomputers 740 Family's software are described below:

- 1) An efficient instruction set and many addressing modes allow the effective use of ROM.
- 2) The same bit management, test, and branch instructions can be performed on the Accumulator, memory, or I/O area.
- 3) Multiple interrupts with separate interrupt vectors allow servicing of different non-periodic events.
- 4) Byte processing and table referencing can be easily performed using the index addressing mode.
- 5) Decimal mode needs no software correction for proper decimal operation.
- 6) The Accumulator does not need to be used in operations using memory and/or I/O.

Accumulator (A) Index Register X (X), Index Register Y (Y)

#### 2. CENTRAL PROCESSING UNIT (CPU)

Six main registers are built into the CPU of the 740 Family.

The Program Counter (PC) is a sixteen-bit register; however, the Accumulator (A), Index Register X (X), Index Register Y (Y), Stack Pointer (S) and Processor Status Register (PS) are eight-bit registers.

Except for the I flag, the contents of these registers are indeterminate after a hardware reset; therefore, initialization is required with some programs (immediately after reset the I flag is set to "1").



Fig.2.1.1 Register Configuration

#### 2.1 Accumulator (A)

The Accumulator, an eight-bit register, is the main register of the microcomputer. This general-purpose register is used most frequently for arithmetic operations, data transfer, temporary memory, conditional judgments, etc.

#### 2.2 Index Register X (X), Index Register Y (Y)

The 740 Family has an Index Register X and an Index Register Y, both of which are eightbit registers.

When using addressing modes which use these index registers, the address, which is added the contents of Index Register to the address specified with operand, is accessed. These modes are extremely effective for referencing subroutine and memory tables.

The index registers also have increment, decrement, compare, and data transfer functions; therefore, these registers can be used as simple accumulators.

#### 2.3 Stack Pointer (S)

The Stack Pointer is an eight-bit register used for generating interrupts and calling subroutines. When an interrupt is received, the following procedure is performed automatically in the indicated sequence:

- The contents of the high-order eight bits of the Program Counter (PCH) are saved to an address using the Stack Pointer contents for the low-order eight bits of the address.
   The Stack Pointer contents are decremented by 1.
- (3) The contents of the low-order eight bits of the Program Counter (PCL) are saved to an address using the Stack Pointer Contents for the low-order eight bits of the address.
   (4) The Stack Pointer contents are decremented by 4
- (4) The Stack Pointer contents are decremented by 1.
- (5) The contents of the Processor Status Register (PS) are saved to an address using the Stack Pointer contents for the low-order eight bits of the address.
- (6) The Stack Pointer contents are decremented by 1.

The Processor Status Register is not saved when calling subroutines (items (5) and (6) above are not executed). The Processor Status Register is saved by executing the PHP instruction in software.

To prevent data loss when generating interrupts and calling subroutines, it is necessary to save other registers as well. This is done by executing the proper instruction in software while in the interrupt service routine or subroutine.

The high-order eight bits of the address are determined by the Stack Page Selection Bit.

For example, the PHA instruction is executed to save the contents of the Accumulator. Executing the PHA instruction saves the Accumulator contents to an address using the Stack Pointer contents as the low-order eight bits of the address.

The RTI instruction is executed to return from an interrupt routine.

When the RTI instruction is executed, the following procedure is performed automatically in sequence.

- (1) The Stack Pointer contents are incremented by 1.
- (2) The contents of an address using the Stack Pointer contents as the low-order eight bits of the address is returned to the Processor Status Register (PS).
- (3) The Stack Pointer contents are incremented by 1.
- (4) The contents of an address using the Stack Pointer as the low-order eight bits of the address is returned to the low-order eight bits of the Program Counter (PCL).
- (5) The Stack Pointer contents are incremented by 1.
- (6) The contents of an address using the Stack Pointer as the low-order eight bits of the address is returned to the high-order eight bits of the Program Counter (PCH).

Steps (1) and (2) are not performed when returning from a subroutine using the RTS instruction. The Processor Status Register should be restored before returning from a subroutine by using the PLP instruction. The Accumulator should be restored before returning from a subroutine or an interrupt servicing routine by using the PLA instruction.

The PLA and PLP instructions increment the Stack Pointer by 1 and return the contents of an address stored in the Stack Pointer to the Accumulator or Processor Status Register, respectively.

Saving data in the stack area gradually fills the RAM area with saved data; therefore, caution must exercised concerning the depth of interrupt levels and subroutine nesting.

#### 2.4 Program Counter (PC)

The Program Counter is a sixteen-bit counter consisting of PCH and PCL, which are each eight-bit registers. The contents of the Program Counter indicates the address which an instruction to be executed next is stored.

The 740 Family uses a stored program system; to start a new operation it is necessary to transfer the instruction and relevant data from memory to the CPU.

Normally the Program Counter is used to indicate the next memory address. After each instruction is executed, the next instruction required is read. This cycle is repeated until the program is finished.

The control of the Program Counter of the 740 Family is almost fully automatic. However, caution must be exercised to avoid differences between program flow and Program Counter contents when using the Stack Pointer or directly altering the contents of the Program Counter.

#### 2.5 Processor Status Register (PS)

The Processor Status Register is an eight-bit register consisting of 5 flags which indicate the status of arithmetic operations and 3 flags which determine operation. Immediately after a reset, only the interrupt disable flag is set to "1," and the other flags are undefined. Therefore, initialize the flags that effect program execution. Especially, initialize the T and D flags because of their effect on operation.

Each of these flags is described below. Table 2.5.1 lists the instructions to set/clear each flag. Refer to the section "Appendix 2 MACHINE LANGUAGE INSTRUCTION TABLE" or "3.3 INSTRUCTIONS" for details on when these flags are altered.

[ Carry flag C ]----- Bit 0 This flag stores any carry or borrow from the Arithmetic Logic Unit (ALU) after an arithmetic operation and is also changed by the Shift or Rotate instruction.

This flag is set by the SEC instruction and is cleared by the CLC instruction.

[ Zero flag Z ] ----- Bit 1

This flag is set when the result of an arithmetic operation or data transfer is "0" and is cleared by any other result.

[Interrupt disable flag I]----- Bit 2 This flag disables interrupts when it is set to "1." This flag immediately becomes "1" when an interrupt is received.

This flag is set by the SEI instruction and is cleared by the CLI instruction.

[ Decimal mode flag D ]----- Bit 3

This flag determines whether addition and subtraction are performed in binary or decimal notation. Addition and subtraction are performed in binary notation when this flag is set to "0" and as a 2-digit, 1-word decimal numeral when set to "1." Decimal notation correction is performed automatically at this time.

This flag is set by the SED instruction and is cleared by the CLD instruction.

Only the ADC and SBC instructions are used for decimal arithmetic operations.

Note that the flags N, V and Z are invalid when decimal arithmetic operations are performed by these instructions.

[Break flag B] ----- Bit 4

This flag determines whether an interrupt was generated with the BRK instruction. When a BRK instruction interrupt occurs, the flag B is set to "1" and saved to the stack; for all other interrupts the flag is set to "0" and saved to the stack.

#### **Processor Status Register (PS)**

<ul> <li>[X modified operation mode flag T] Bit 5</li> <li>This flag determines whether arithmetic operations are performed via the Accumulator or directly on a memory location. When the flag is set to "0", arithmetic operations are performed between the Accumulator and memory. When "1", arithmetic operations are performed directly on a memory location.</li> <li>This flag is set by the SET instruction and is cleared by the CLT instruction.</li> <li>(1) When the T flag = 0</li> </ul>
$A \leftarrow A * M2$
* : indicates an arithmetic operation
A: accumulator contents
M2: contents of a memory location specified by the addressing mode of the arithmetic operation
(2) When the T flag = 1
M1 ← M1 * M2
* : indicates arithmetic operation
M1: contents of a memory location, designated by the contents of Index Register X.
M2: contents of a memory location specified by the addressing mode of arithmetic operation.
[ Overflow flag V ] Bit 6
This flag is set to "1" when an overflow occurs as a result of a signed arithmetic operation. An overflow occurs when the result of an addition or subtraction exceeds +127 (7F16) or $-128$ (8016) respectively.
The CLV instruction clears the Overflow Flag. There is no set instruction
The overflow flag is also set during the BIT instruction when bit 6 of the value being tested is "1."
Overflows do not occur when the result of an addition or subtraction is equal to or smaller than the above numerical values, or for additions involving values with different signs.
[Negative flag N]Bit 7
This flag is set to match the sign bit (bit 7) of the result of a data or arithmetic operation.
This flag can be used to determine whether the results of arithmetic operations are positive
or negative, and also to perform a simple bit test.

	Flag C	Flag Z	Flag I	Flag D	Flag B	Flag T	Flag V	Flag N
Set instruction	SEC		SEI	SED		SET		
Clear instruction	CLC		CLI	CLD		CLT	CLV	

#### Table 2.5.1 Instructions to set/clear each flag of processor status register

#### 3. INSTRUCTIONS

#### 3.1 Addressing Mode

The 740 Family has 19 addressing modes and a powerful memory access capability. When extracting data required for arithmetic and logic operations from memory or when storing the results of such operations in memory, a memory address must be specified. The specification of the memory address is called addressing. The data required for addressing and the registers involved are described below. The 740 Family instructions can be classified into three kinds, by the number of bytes required in program memory for the instruction: 1-byte, 2-byte and 3-byte instructions. In each case, the first byte is known as the "Op-Code (operation code)" which forms the basis of the instruction. The second or third byte is called the "oper-and" which affects the addressing. The contents of index registers X and Y can also effect the addressing.



Fig.3.1.1 Byte Structure of Instructions

Although there are many addressing modes, there is always a particular memory location specified. What differs is whether the operand, or the index register contents, or a combination of both should be used to specify the memory or jump destination. Based on these 3 types of instructions, the range of variation is increased and operation is enhanced by combinations of the bit operation instructions, jump instruction, and arithmetic instructions.

As for 1-byte instruction, an accumulator or a register is specified, so that the instruction does not have "operand," which specify memory.

# Immediate

Addressing mode

#### Addressing mode : Immediate

Function : Specifies the Operand as the data for the instruction.

Instructions : ADC, AND, CMP, CPX, CPY, EOR, LDA, LDX, LDY, ORA, SBC

Example : MnemonicMachine code $\Delta ADC \Delta \# $A5$ 6916 A516TT

This symbol(#) indicates the Immediate addressing mode.



#### Addressing mode : Accumulator

- Function : Specifies the contents of the Accumulator as the data for the instruction.
- Instructions : ASL, DEC, INC, LSR, ROL, ROR

Example : Mnemonic **AROLAA**  Machine code 2A16



Zero Page

Addressing mode

Addressing mode : Zero Page

- Function : Specifies the contents in a Zero Page memory location as the data for the instruction. The address in the Zero Page memory location is determined by using Operand as the low-order byte of the address and 0016 as the high-order byte.
- Instructions : ADC, AND, ASL, BIT, CMP, COM, CPX, CPY, DEC, EOR, INC, LDA, LDM, LDX, LDY, LSR, ORA, ROL, ROR, RRF, SBC, STA, STX, STY, TST

Example : Mnemonic Machine code <u>AADC</u>A\$40 6516 4016



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Addressing mode : Zero Page X

Function : Specified the contents in a Zero Page memory location as the data for the instruction. The address in the Zero Page memory location is determined by the following:

- (a) Operand and the Index Register X are added. (If as a result of this addition a carry occurs, it is ignored.)
- (b) The result of the addition is used as the low-order byte of the address and 0016 as the high-order byte.
- Instructions : ADC, AND, ASL, CMP, DEC, DIV, EOR, INC, LDA, LDY, LSR, MUL, ORA, ROL, ROR, SBC, STA, STY

Example : Mnemonic <u>AADCA</u>\$5E,X Machine code 7516 5E16



Zero Page Y

Addressing mode

Addressing mode : Zero Page Y

Function : Specifies the contents in a Zero Page memory location as the data for the instruction. The address in the Zero Page memory location is determined by the following:

- (a) Operand and the Index Register Y are added (if as a result of this addition a carry occurs, it is ignored).
- (b) The result of the addition is used as the low-order byte of the address and 0016 as the high-order byte.

Instructions :LDX, STX

Example :Mnemonic **ΔLDXΔ\$62,Y**  Machine code B616 6216



Absolute

#### Addressing mode : Absolute

- Function : Specifies the contents in a memory location as the data for the instruction. The address in the memory location is determined by using Operand I as the loworder byte of the address and Operand II as the highorder byte.
- Instructions : ADC, AND, ASL, BIT, CMP, CPX, CPY, DEC, EOR, INC, JMP, JSR, LDA, LDX, LDY, LSR, ORA, ROL, ROR, SBC, STA, STX, STY

Example : Mnemonic ΔΑDCΔ\$AD12 Machine code 6D16 1216 AD16



# Absolute X

#### Addressing mode : Absolute X

- Function : Specifies the contents in a memory location as the data for the instruction. The address in the memory location is determined by the following:
  - (a) Operand I is used as the low-order byte of an address, Operand II as the high-order byte.
  - (b) Index Register X is added to the address above. The result is the address in the memory location.
- Instructions : ADC, AND, ASL, CMP, DEC, EOR, INC, LDA, LDY, LSR, ORA, ROL, ROR, SBC, STA

Example : Mnemonic Machine code ΔΑΟCΔ\$ΑΟ12, Χ 7D16 1216 ΑΟ16



Absolute Y

#### Addressing mode : Absolute Y

Function : Specifies the contents in a memory location as the data for the instruction. The address in the memory location is determined by the following:

- (a) Operand I is used as the low-order byte of an address, Operand II as the high-order byte.
- (b) Index Register Y is added to the address above. The result is the address in the memory location.

Instructions : ADC, AND, CMP, EOR, LDA, LDX, ORA, SBC, STA

Example : Mnemonics

 monics
 Machine code

 ΔΑDCΔ\$AD12, Y
 7916 1216 AD16



Implied

Addressing mode

#### Addressing mode : Implied

- Function : Operates on a given register or the Accumulator, but the address is always inherent in the instruction.
- Instructions : BRK, CLC, CLD, CLI, CLT, CLV, DEX, DEY, INX, INY, NOP, PHA, PHP, PLA, PLP, RTI, RTS, SEC, SED, SEI, SET, STP, TAX, TAY, TSX, TXA, TXS, TYA, WIT

Example : MnemonicMachine codeΔCLC1816



#### Addressing mode : **Relative**

Function : Specifies the address in a memory location where the next Op-Code is located.
When the branch condition is satisfied, Operand and the Program Counter are added. The result of this addition is the address in the memory location.
When the branch condition is not satisfied, the next instruction is executed.

Instructions : BCC, BCS, BEQ, BMI, BNE, BPL, BRA, BVC, BVS



**Indirect X** 

Addressing mode : Indirect X

Function : Specifies the contents in a memory location as the data for the instruction. The address in the memory location is determined by the following:

- (a) A Zero Page memory location is determined by the adding the Operand and Index Register X (if as a result of this addition a carry occurs, it is ignored).
- (b) The result of the addition is used as the low-order byte of an address in the Zero Page memory location and 0016 as the high-order byte.
- (c) The contents of the address in the Zero Page memory location is used as the low-order byte of the address in the memory location.
- (d) The next Zero Page memory location is used as the high-order byte of the address in the memory location.

Instructions : ADC, AND, CMP, EOR, LDA, ORA, SBC, STA

Example :Mnemonic ΔΑDCΔ(\$1E,X) Machine code 6116 1E16



Assuming that "0016" for Data I, and "1416" for Data II are stored in advance.

**Indirect** Y

Addressing mode : Indirect Y

- Function : Specifies the contents in a memory location as the data for the instruction. The address in the memory location is determined by the following:
  - (a) The Operand is used the low-order byte of an address in the Zero Page memory location and 0016 of the high-order byte.
  - (b) The contents of the address in the Zero Page memory location is used as the low-order byte of an address. The next Zero Page memory location is used as the high-order byte.
  - (c) The Index Register Y is added to the address in Step b. The result of this addition is the address in the memory location.

#### Instructions : ADC, AND, CMP, EOR, LDA, ORA, SBC, STA

Example : Mnemonic

Machine code 7116 1E16



Assuming that "0116" for Data I, and "1216" for Data II are stored in advance.

# INSTRUCTIONS Indirect Absolute Addressing mode

#### Addressing mode : Indirect Absolute

Function : Specifies the address in a memory location as the jump destination address.

The address in the memory location is determined by the following:

- (a) Operand I is used as the low-order byte of an address and Operand II as the high-order byte.
- (b) The contents of the address above is used as the low-order byte and the contents of the next address as the high-order byte.
- (c) The high-order and low-order bytes in step b together form the address in the memory location.

Instructions : JMP

Example : Mnemonic ΔJMPΔ(\$1400) Machine code 6C16 0016 1416



Assuming that "FF16" for Data I, and "1E16" for Data II are stored in advance.

Note: The page's last address (address XXFF16) cannot be specified for the indirect designation address; in other words, JMP (\$XXFF) cannot be executed.

RENESAS

# Zero Page Indirect Addressing mode

Addressing mode : Zero Page Indirect Absolute

- Function : Specifies the address in a memory location as the jump destination address. The address in the memory location is determined by the following:
  - (a) Operand is used as the low-order byte of an address in the Zero Page memory location and 0016 as the high-order byte.
  - (b) The contents of the address in the Zero Page memory location is used as the low-order byte and the contents of the next Zero Page memory location as high-order byte.
  - (c) The high-order and low-order bytes in step b together form the address of the memory location.

Instructions : JMP, JSR

Example : Mnemonic **ΔJMPΔ(\$45)**  Machine code B216 4516



Assuming that "FF16" for Data I, and "1E16" for Data II are stored in advance.

**Special Page** 

Addressing mode

#### Addressing mode : Special Page

Function : Specifies the address in a Special Page memory location as the jump destination address. The address in the Special Page memory location is determined by using Operand as the low-order byte of the address and FF16 as the high-order byte.





Zero Page Bit

Addressing mode

Addressing mode : Zero Page Bit

Function : Specifies one bit of the contents in a Zero Page memory location as the data for the instruction. Operand is used as the low-order byte of the address in the Zero Page memory location and 0016 as the high-order byte. The bit position is designated by the high-order three bits of the Op-code.

Instructions : CLB, SEB

Example : Mnemonic <u>ACLBA5</u>,\$44

Machine code BF16 4416



### INSTRUCTIONS Accumulator Bit Addressing mode

Addressing mode : Accumulator Bit

Function : Specifies one bit of the Accumulator as the data for the instruction. The bit position is designated by the high-order three bits of the Op-Code.

Instruction: CLB, SEB

Example :Mnemonic ΔCLBΔ5,A Machine code BB16

#### Accumulator





#### INSTRUCTIONS Accumulator Bit Relative Addressing mode

Addressing mode : Accumulator Bit Relative

Function :Specifies the address in a memory location where the next Op-Code is located. The bit position is designated by the high-order three bits of the Op-Code. If the branch condition is satisfied, Operand and the Program Counter are added. The result of this addition is the address in the memory location. When the branch condition is not satisfied, the next instruction is executed.

Instructions :BBC, BBS Example : Mnemonic Machine code B316 F216 ∆BBC∆5,A,\*–12 Decimal When the bit 5 of the When the bit 5 of the Accumulator is cleared Accumulator is set Accumulator Accumulator bit 5 bit 5 1 0 Memory Memory Address to be -12 executed next Bit designation Bit designation Op-code(B316) Op-code(B316) Jump Operand (F216) Operand (F216) Address to be \* +2 +2 executed next

RENESAS

#### INSTRUCTIONS Zero Page Bit Relative Addressing mode

Addressing mode : Zero Page Bit Relative

Function : Specifies the address of a memory location where the next Op-Code is located.
The bit position is designated by the high-order three bits of the Op-Code. The address in the Zero Page memory location is determined by using Operand I as low-order byte of the address and 0016 as the high-order byte. If the branch condition is satisfied, Operand II and the Program Counter are added. The result of this addition is the address in the memory location. When the branch condition is not satisfied, the next instruction is executed.

Instructions : BBC, BBS



RENESAS

#### 3.2 Instruction Set

The 740 Family has 71 types of instructions. The detailed explanation of the instructions is presented in §3.3. Note that some instructions cannot be used for some products.

#### 3.2.1 Data transfer instructions

These instructions transfer the data between registers, register and memory, and memories. The following are data transfer instructions.

	Instruction	Function					
	LDA	Load memory value into Accumulator, or memory					
		where is indicated by Index Register X					
Load	LDM	Load immediate value into memory					
	LDX	Load memory contents into Index Register X					
	LDY	Load memory contents into Index Register Y					
	STA	Store Accumulator into memory					
Store	STX	Store Index Register X into memory					
	STY	Store Index Register Y into memory					
	TAX	Transfer Accumulator to the Index Register X					
	TXA	Transfer Index Register X into the Accumulator					
Transfor	TAY	Transfer Accumulator into the Index Register Y					
Transier	TYA	Transfer Index Register Y into the Accumulator					
	TSX	Transfer Stack Pointer into the Index Register X					
	TXS	Transfer Index Register X into the Stack Pointer					
	PHA	Push Accumulator onto the Stack					
Stack	PHP	Push Processor Status onto the Stack					
Operation	PLA	Pull Accumulator from the Stack					
-	PLP	Pull Processor Status from the Stack					

#### 3.2.2 Operating instruction

The operating instructions include the operations of addition and subtraction, logic, comparison, rotation, and shift.

The operating instructions are as follows:

	Instructions	Contents		
	ADC	Add memory contents and C flag to Accumulator or memory		
		where is indicated by Index Register X		
	SBC	Subtracts memory contents and C flag's complement from		
		Accumulator or memory where is indicated by Index		
Addition		Register X		
&	INC	Increment Accumulator or memory contents by 1		
Subtraction	DEC	Decrement Accumulator or memory contents by 1		
	INX	Increment Index Register X by 1		
	DEX	Decrement Index Register X by 1		
	INY	Increment Index Register Y by 1		
	DEY	Decrement Index Register Y by 1		
	MUL(Note)	Multiply Accumulator with memory specified by Zero Page		
Multiplication		X addressing mode and store high-order byte of result on		
&		Stack and low-order byte in Accumulator		
Division	DIV(Note)	Quotient is stored in Accumulator and one's complement of		
		remainder is pushed onto stack		
	AND	"AND" memory with Accumulator or memory where is		
		indicated by Index Register X		
	ORA	"OR" memory with Accumulator or memory where is		
		indicated by Index Register X		
Logical	EOR	"Exclusive-OR" memory with Accumulator or memory where		
Operation		is indicated by Index Register X		
	COM	Store one's complement of memory contents to memory		
	BIT	"AND" memory with Accumulator (The result is not stored		
		into anywhere.)		
	TST	Test whether memory content is "0" or not		
	CMP	Compare memory contents and Accumulator or memory		
Comparison		where is indicated by Index Register X		
	CPX	Compare memory contents and Index Register X		
	CPY	Compare memory contents and Index Register Y		
	ASL	Shift left one bit (memory contents or Accumulator)		
01.74	LSR	Shift right one bit (memory contents or Accumulator)		
Shift	ROL	Rotate one bit left with carry (memory contents or		
Č Detete		Accumulator)		
Rotate	ROR	Rotate one bit right with carry (memory contents or		
		Accumulator)		
	RRF	Rotate four bits right witout carry (memory)		

**Note:** For some products, multiplication and division instructions cannot be used.

#### 3.2.3 Bit managing instructions

The bit managing instructions clear "0" or set "1" designated bits of the Accumulator or memory.

	Instructions	Contents	
Bit	CLB	Clear designated bit in the Accumulator or memory	
Managing	SEB	Set designated bit in the Accumulator or memory	

#### 3.2.4 Flag setting instructions

The flag setting instructions clear "0" or set "1" C, D, I, T and V flags.

	Instructions	Contents		
Flag Setting	CLC	Clear C flag		
	SEC	Set C flag	C liay . Carly Flag	
	CLD	Clear D flag	D flag : Decimal Mode Flag	
	SED	Set D flag		
	CLI	Clear I flag	I flag : Interrupt Disable Flag	
	SEI	Set I flag		
	CLT	Clear T flag	T flag : X Modified Operation Mode Flag	
	SET	Set T flag		
	CLV	Clear V flag	V flag : Overflow Flag	

#### 3.2.5 Jump, Branch and Return instructions

The jump, branch and return instructions as following are used to change program flow.

	Instructions	Contents			
Jump	JMP	Jump to new location			
	BRA	Jump to new location			
	JSR	Jump to new location saving the current address			
Branch	BBC	Branch when the designated bit in the Accumulator or memory is "0"			
	BBS	Branch when the designated bit in the Accumulator or memory is "1"			
	BCC	Branch when the C Flag is "0"	C flag · Carry Flag		
	BCS	Branch when the C Flag is "1"	o hag i oarry r hag		
	BNE	Branch when the Z Flag is "0"	Z flag : Zero Flag		
	BEQ	Branch when the Z Flag is "1"			
	BPL	Branch when the N Flag is "0"	N flag : Negative Flag		
	BMI	Branch when the N Flag is "1"			
	BVC	Branch when the V Flag is "0"	V flag : Overflow Flag		
	BVS	Branch when the V Flag is "1"	i nog i er en en eng		
Return	RTI	Return from interrupt			
	RTS	Return from subroutine			
### **INSTRUCTIONS**

### 3.2.6 Interrupt instruction (Break instruction)

This instruction causes a software interrupt.

	Instruction	Contents
Interrupt	BRK	Executes a software interrupt.

#### 3.2.7 Special instructions

These special instructions control the oscillation and the internal clock.

	Instructions	Contents
	WIT	Stops the internal clock.
Special	STP	Stops the oscillation of oscillator.

#### 3.2.8 Other instruction

	Instruction	Contents
Other	NOP	Only advances the program counter.

#### 3.3 Description of instructions

This section presents in detail the 740 Family instructions by arranging mnemonics of instructions alphabetically and dividing each instruction essentially into one page.

The heading of each page is a mnemonic. Operation, explanation and changes of status flags are indicated for each instruction. In addition, assembler coding format, machine code, byte number, and list of cycle numbers for each addressing mode are indicated. The following are symbols used in this manual:

Symbol	Description	Symbol	Description
А	Accumulator	hh	Address high-order byte data
Ai	Bit i of Accumulator		in 0 to 255
PC	Program Counter	II	Address low-order byte data
PC∟	Low-order byte of Program		in 0 to 255
	Counter	ZZ	Zero page address data in 0
РСн	High-order byte of Program		to 255
	Counter	nn	Data in 0 to 255
PS	Processor Status Register	i	Data in 0 to 7
S	Stack Pointer	*	Contents of the Program
Х	Index Register X		Counter
Y	Index Register Y	$\Delta$	Tab or space
М	Memory	#	Immediate mode
Mi	Bit i of memory	\	Special page mode
С	Carry Flag	\$	Hexadecimal symbol
Z	Zero Flag	+	Addition
I	Interrupt Disable Flag	-	Subtraction
D	Decimal Operation Mode Flag	X	Multiplication
В	Break Flag	/	Division
Т	X Modified Operations Mode	^	Logical AND
	Flag	$\vee$	Logical OR
V	Overflow Flag	$\forall$	Logical exclusive OR
N	Negative Flag	()	Contents of register, memory,
REL	Relative address		etc.
BADRS	Break address	$\leftarrow$	Direction of data transfer

### **AD**D WITH **C**ARRY

- **Operation**: When (T) = 0,  $(A) \leftarrow (A) + (M) + (C)$ (T) = 1,  $(M(X)) \leftarrow (M(X)) + (M) + (C)$
- Function : When T = 0, this instruction adds the contents M, C, and A; and stores the results in A and C. When T = 1, this instruction adds the contents of M(X), M and

C; and stores the results in M(X) and C. When T=1, the contents of A remain unchanged, but the contents of status flags are changed.

ADC

M(X) represents the contents of memory where is indicated by X.

- Status flag: N: N is 1 when bit 7 is 1 after the operation; otherwise it is 0.
  - V: V is 1 when the operation result exceeds +127 or |-128; otherwise it is 0.
  - T: No change
  - **B**: No change
  - I: No change
  - **D**: No change
  - **Z**: Z is 1 when the operation result is 0; otherwise it is 0.
  - **C**: C is 1 when the result of a binary addition exceeds 255 or when the result of a decimal addition exceeds 99; otherwise it is 0.

Addressing mode	Statement	Machine codes	Byte number	Cycle number
Immediate	∆ADC∆#\$nn	6916, nn16	2	2
Zero page	∆ADC∆\$zz	6516, zz16	2	3
Zero page X	∆ADC∆\$zz,X	7516, zz16	2	4
Absolute	∆ADC∆\$hhll	6D16, ll16, hh16	3	4
Absolute X	∆ADC∆\$hhll,X	7D16, ll16, hh16	3	5
Absolute Y	∆ADC∆\$hhll,Y	7916, ll16, hh16	3	5
(Indirect X)	$\Delta ADC \Delta (\$zz, X)$	6116, zz16	2	6
(Indirect Y)	ΔADCΔ(\$zz),Υ	7 <b>1</b> 16, ZZ16	2	6

Notes 1: When T=1, add 3 to the cycle number.

2: When ADC instruction is executed in decimal operation mode (D = 1), execute at least one instruction after the ADC instruction before executing a SEC, CLC, or CLD instruction.

In decimal operation mode, the N, V, Z flags are invalid.

## AND

## AND

### LOGICAL AND

- Operation : When (T) = 0, (A)  $\leftarrow$  (A)  $\land$  (M) (T) = 1, (M(X))  $\leftarrow$  (M(X))  $\land$  (M)
- Function : When T = 0, this instruction transfers the contents of A and M to the ALU which performs a bit-wise AND operation and stores the result back in A.

When T = 1, this instruction transfers the contents M(X) and M to the ALU which performs a bit-wise AND operation and stores the results back in M(X). When T = 1 the contents of A remain unchanged, but status flags are changed.

M(X) represents the contents of memory where is indicated by X.

### Status flag: N: N is 1 when bit 7 is 1 after the operation; otherwise it is 0.

- V: No change
- T: No change
- **B**: No change
- I: No change
- D: No change
- **Z**: Z is 1 when the operation result is 0; otherwise it is 0.
- C: No change

Addressing mode	Statement	Machine codes	Byte number	Cycle number
Immediate	∆AND∆#\$nn	2916, nn16	2	2
Zero page	∆AND∆\$zz	2516, ZZ16	2	3
Zero page X	∆AND∆\$zz,X	3516, zz16	2	4
Absolute	∆AND∆\$hhll	2D16, ll16, hh16	3	4
Absolute X	∆AND∆\$hhll,X	3D16, ll16, hh16	3	5
Absolute Y	∆AND∆\$hhll,Y	3916, ll16, hh16	3	5
(Indirect X)	$\Delta AND\Delta(\$zz,X)$	2116, zz16	2	6
(Indirect Y)	$\Delta AND\Delta(\$zz), Y$	<b>31</b> 16, <b>ZZ</b> 16	2	6

Note: When T = 1, add 3 to a cycle number.



- B: No change
- I: No change
- D: No change
- **Z**: Z is 1 when the operation result is 0; otherwise it is 0.
- **C**: C is 1 when bit 7 of A or M is 1, before this operation; otherwise it is 0.

Addressing mode	Statement	Machine codes	Byte number	Cycle number
Accumulator	ΔΑSLΔΑ	0A16	1	2
Zero page	∆ASL∆\$zz	0616, ZZ16	2	5
Zero page X	∆ASL∆\$zz,X	<b>16</b> 16, <b>ZZ</b> 16	2	6
Absolute	∆ASL∆\$hhll	0E16, II16, hh16	3	6
Absolute X	∆ASL∆\$hhll,X	1E16, II16, hh16	3	7

### BBC

### BRANCH ON BIT CLEAR

### **Operation :** When (Mi) or (Ai) = 0, (PC) $\leftarrow$ (PC) + n + REL

- (Mi) or (Ai) = 1, (PC)  $\leftarrow$  (PC) + n
  - n: If addressing mode is Zero Page Bit Relative, n=3. And if addressing mode is Accumulator Bit Relative, n=2.
- **Function :** This instruction tests the designated bit i of M or A and takes a branch if the bit is 0. The branch address is specified by a relative address. If the bit is 1, next instruction is executed.

Status flag : No change

Addressing mode	Statement	Machine codes	Byte number	Cycle number
Accumulator bit		(201+13)16 rr16	0	1
Relative		(201+13)10, 1110	Z	4
Zero page bit	ABBCAi \$77 \$6611	(20i+17)16,	3	5
Relative	ΔΟΟζΔι,φΖΖ,φΓΙΓΙΙΙ	<b>ZZ</b> 16, <b>ľľ</b> 16	5	5

Notes 1: rr16=\$hhll-(\*+n). The rr16 is a value in a range of -128 to +127. 2: When a branch is executed, add 2 to the cycle number.

3: When executing the BBC instruction after the contents of the interrupt request bit is changed, one instruction or more must be passed before the BBC instruction is executed.

### BRANCH ON BIT SET

- (Mi) or (Ai) = 0, (PC)  $\leftarrow$  (PC) + n
  - n : If addressing mode is Zero Page Bit Relative, n=3. And if addressing mode is Accumulator Bit Relative, n=2.

BBS

**Function :** This instruction tests the designated bit i of the M or A and takes a branch if the bit is 1. The branch address is specified by a relative address. If the bit is 0, next instruction is executed.

Status flag : No change

Addressing mode	Statement	Machine codes	Byte number	Cycle number
Accumulator bit	∆BBS∆i,A,\$hhll	(20i+3)16, rr16	2	4
Zero page bit	∆BBS∆i,\$zz,\$hhll	(201+7)16,	3	5
Relative	<i>,,</i>	ZZ16, ľľ16	-	-

Notes 1:  $rr_{16}=$  hll-(\*+n). The rr\_{16} is a value in a range of -128 to +127. 2: When a branch is executed, add 2 to the cycle number.

3: When executing the BBS instruction after the contents of the interrupt request bit is changed, one instruction or more must be passed before the BBS instruction is executed.

## BCC

### BRANCH ON CARRY CLEAR

### **Operation** : When (C) = 0, (PC) $\leftarrow$ (PC) + 2 + REL (C) = 1, (PC) $\leftarrow$ (PC) + 2

**Function** : This instruction takes a branch to the appointed address if C is 0. The branch address is specified by a relative address. If C is 1, the next instruction is executed.

Status flag : No change

Addressing mode	Statement	Machine codes	Byte number	Cycle number
Relative	∆BCC∆\$hhll	9016, rr16	2	2

### **B**RANCH ON **C**ARRY **S**ET

BCS

**Operation :** When (C) = 1, (PC)  $\leftarrow$  (PC) + 2 + REL (C) = 0, (PC)  $\leftarrow$  (PC) + 2

**Function :** This instruction takes a branch to the appointed address if C is 1. The branch address is specified by a relative address. If C is 0, the next instruction is executed.

Status flag : No change

Addressing mode	Statement	Machine codes	Byte number	Cycle number
Relative	∆BCS∆\$hhll	B016, rr16	2	2



### BRANCH ON EQUAL

BEC

**Operation :** When (Z) = 1,  $(PC) \leftarrow (PC) + 2 + REL$ (Z) = 0,  $(PC) \leftarrow (PC) + 2$ 

Function : This instruction takes a branch to the appointed address when Z is 1. The branch address is specified by a relative address. If Z is 0, the next instruction is executed.

Status flag : No change

Addressing mode	Statement	Machine codes	Byte number	Cycle number
Relative	∆BEQ∆\$hhll	F016,rr16	2	2

# BIT TEST BIT IN MEMORY WITH ACCUMULATOR BIT

**Operation** :  $(A) \land (M)$ 

**Function :** This instruction takes a bit-wise logical AND of A and M contents; however, the contents of A and M are not modified. The contents of N, V, Z are changed, but the contents of A, M remain unchanged.

### Status flag: N:N is 1 when bit 7 of M is 1; otherwise it is 0.

- V: V is 1 when bit 6 of M is 1; otherwise it is 0.
  - T: No change
  - **B**: No change
  - I: No change
  - **D**: No change
  - **Z**: Z is 1 when the result of the operation is 0; otherwise Z is 0.
  - C: No change

Addressing mode	Statement	Machine codes	Byte number	Cycle number
Zero page	ΔBITΔ\$zz	2416, ZZ16	2	3
Absolute	∆BIT∆\$hhll	2C16, II16, hh16	3	4



### BRANCH ON RESULT MINUS

BMI

### Operation : When (N) = 1, (PC) $\leftarrow$ (PC) + 2 + REL (N) = 0, (PC) $\leftarrow$ (PC) + 2

Function : This instruction takes a branch to the appointed address when N is 1. The branch address is specified by a relative address. If N is 0, the next instruction is executed.

Status flag : No change

Addressing mode	Statement	Machine codes	Byte number	Cycle number
Relative	∆BMI∆\$hhll	3016, rr16	2	2

### BRANCH ON NOT EQUAL

**BNE** 

### **Operation :** When (Z) = 0, $(PC) \leftarrow (PC) + 2 + REL$ (Z) = 1, $(PC) \leftarrow (PC) + 2$

**Function :** This instruction takes a branch to the appointed address if Z is 0. The branch address is specified by a relative address. If Z is 1, the next instruction is executed.

Status flag : No change

Addressing mode	Statement	Machine codes	Byte number	Cycle number
Relative	∆BNE∆\$hhll	D016, rr16	2	2

### **B**RANCH ON RESULT **PL**US

**BPL** 

### Operation : When (N) = 0, (PC) $\leftarrow$ (PC) + 2 + REL (N) = 1, (PC) $\leftarrow$ (PC) + 2

**Function** : This instruction takes a branch to the appointed address if N is 0. The branch address is specified by a relative address. If N is 1, the next instruction is executed.

Status flag : No change

Addressing mode	Statement	Machine codes	Byte number	Cycle number
Relative	∆BPL∆\$hhll	<b>10</b> 16, <b>rr</b> 16	2	2

### **Operation** : (PC) $\leftarrow$ (PC) + 2 + REL

**Function** : This instruction branches to the appointed address. The branch address is specified by a relative address.

Status flag : No change

Addressing mode	Statement	Machine codes	Byte number	Cycle number
Relative	∆BRA∆\$hhll	8016, rr16	2	4

Note:  $rr_{16}=$  hll-(\*+2). The rr\_{16} is a value in a range of -128 to +127.

## BRK

FORCE **BR**EAK

**Function :** When the BRK instruction is executed, the CPU pushes the current PC contents onto the stack. The BADRS designated in the interrupt vector table is stored into the PC.

Status flag: N: No change V: No change T: No change

- **B**:1
- **I**: 1
- **D**: No change
- Z: No change
- C: No change

Addressing mode	Statement	Machine codes	Byte number	Cycle number
Implied	ΔΒRΚΔ	0016	1	7

Notes 1: "BADRS" means a break address.

- 2: The value of the PC pushed onto the stack by the execution of the BRK instruction is the BRK instruction address plus two. Therefore, the byte following the BRK will not be executed when the value of the PC is returned from the BRK routine.
- 3: Both after the BRK instruction is executed and after INT is input, the program is branched to the address where is specified by the interrupt vector table. By testing the value of the B Flag in the PS (pushed on the Stack) in the interrupt service routine, the user can determine if the interrupt was caused by the BRK instruction.

### **B**RANCH ON OVERFLOW **C**LEAR

BVC

Operation : When (V) = 0, (PC)  $\leftarrow$  (PC) + 2 + REL (V) = 1, (PC)  $\leftarrow$  (PC) + 2

Function : This instruction takes a branch to the appointed address if V is 0. The branch address is specified by a relative address. If V is 1, the next instruction is executed.

Status flag : No change

Addressing mode	Statement	Machine codes	Byte number	Cycle number
Relative	∆BVC∆\$hhll	5016, rr16	2	2

## BVS

### BRANCH ON OVERFLOW SET

**Operation** : When (V) = 1,  $(PC) \leftarrow (PC) + 2 + REL$ (V) = 0,  $(PC) \leftarrow (PC) + 2$ 

Function : This instruction takes a branch to the appointed address when V is 1. The branch address is specified by a relative address. When V is 0, the next instruction is executed.

Status flag : No change

Addressing mode	Statement	Machine codes	Byte number	Cycle number
Relative	∆BVS∆\$hhll	7016, rr16	2	2

## CLB

Function : This instruction clears the designated bit i of A or M.

Status flag : No change

Addressing mode	Statement	Machine codes	Byte number	Cycle number
Accumulator bit	∆CLB∆i,A	(20i+1B)16	1	2
Zero page bit	∆CLB∆i,\$zz	(20i+1F)16, ZZ16	2	5

## CLC

**Operation** :  $(C) \leftarrow 0$ 

Function : This instruction clears C.

Status flag: N: No change V: No change T: No change B: No change I: No change D: No change Z: No change

**C**: 0

Addressing mode	Statement	Machine codes	Byte number	Cycle number
Implied	∆CLC	<b>18</b> 16	1	2

## CLD

**Operation** :  $(D) \leftarrow 0$ 

Function : This instruction clears D.

Status flag: N: No change V: No change T: No change B: No change I: No change D: 0 Z: No change C: No change

Addressing mode	Statement	Machine codes	Byte number	Cycle number
Implied	ΔCLD	D816	1	2

# CLEAR INTERRUPT DISABLE STATUS

**Operation** : (I)  $\leftarrow 0$ 

Function : This instruction clears I.

Status flag: N: No change

- V: No change
- T: No change
- B: No change
- I: 0
- **D**: No change
- Z: No change
- C: No change

Addressing mode	Statement	Machine codes	Byte number	Cycle number
Implied	ΔCLI	5816	1	2

## CLT

**Operation** :  $(T) \leftarrow 0$ 

Function : This instruction clears T.

Status flag:N : No changeV : No changeT : 0B : No changeI : No changeD : No changeZ : No changeC : No change

Addressing mode	Statement	Machine codes	Byte number	Cycle number
Implied		<b>12</b> 16	1	2

## CLV

**Operation** :  $(V) \leftarrow 0$ 

Function : This instruction clears V.

Status flag N: No change V: 0 T: No change B: No change I: No change

**D**: No change

Z: No change

 $\boldsymbol{C}$  : No change

Addressing mode	Statement	Machine codes	Byte number	Cycle number
Implied	ΔCLV	B816	1	2

## CMP

### **C**O**MP**ARE

CMP

- **Operation :** When (T) = 0, (A) (M)(T) = 1, (M(X)) - (M)
- Function : When T = 0, this instruction subtracts the contents of M from the contents of A. The result is not stored and the contents of A or M are not modified. When T = 1, the CMP subtracts the contents of M from the contents of M(X). The result is not stored and the contents of M(X), M, and A are not modified. M(X) represents the contents of memory where is indicated by X.
- Status flag: N: N is 1 when bit 7 of the operation result is 1 after the operation; otherwise N is 0.
  - V: No change
  - T: No change
  - B: No change
  - I: No change
  - **D**: No change
  - **Z**: Z is 1 when the operation result is 0; otherwise Z is 0.
  - **C**: C is 1 when the subtracted result is equal to or greater than 0; otherwise C is 0.

Addressing mode	Statement	Machine codes	Byte number	Cycle number
Immediate	∆CMP∆#\$nn	C916, nn16	2	2
Zero page	∆CMP∆\$zz	C516, ZZ16	2	3
Zero page X	∆CMP∆\$zz,X	D516, zz16	2	4
Absolute	∆CMP∆\$hhll	CD16, ll16, hh16	3	4
Absolute X	∆CMP∆\$hhll,X	DD16, II16, hh16	3	5
Absolute Y	∆CMP∆\$hhll,Y	D916, ll16, hh16	3	5
(Indirect X)	∆CMP∆(\$zz,X)	C116, ZZ16	2	6
(Indirect Y)	ΔCMPΔ(\$zz),Υ	D116, ZZ16	2	6

Note: When T=1, add 1 to the cycle number.

## COM

COM

### **COM**PLEMENT

**Operation** :  $(M) \leftarrow \overline{(M)}$ 

**Function :** This instruction takes the one's complement of the contents of M and stores the result in M.

- V: No change
- T: No change
- B: No change
- I: No change
- **D**: No change
- **Z**: Z is 1 when the operation result is 0; otherwise Z is 0.
- C: No change

Addressing mode	Statement	Machine codes	Byte number	Cycle number
Zero page	∆COM∆\$zz	4416, ZZ16	2	5

**Operation** : (X) - (M)

- Function : This instruction subtracts the contents of M from the contents of X. The result is not stored and the contents of X and M are not modified.
- Status flag: N: N is 1 when bit 7 of the operation result is 1 after the operation; otherwise N is 0.
  - V: No change
  - T: No change
  - **B**: No change
  - I: No change
  - **D**: No change
  - **Z**: Z is 1 when the operation result is 0; otherwise Z is 0.
  - **C**: C is 1 when the subtracted result is equal to or greater than 0; otherwise C is 0.

Addressing mode	Statement	Machine codes	Byte number	Cycle number
Immediate	∆CPX∆#\$nn	E016, nn16	2	2
Zero page	ΔCPXΔ\$zz	E416, ZZ16	2	3
Absolute	∆CPX∆\$hhll	EC16, II16, hh16	3	4

**Operation** : (Y) - (M)

- **Function :** This instruction subtracts the contents of M from the contents of Y. The result is not stored and the contents of Y and M are not modified.
- Status flag: N: N is 1 when bit 7 of the operation result is 1 after the operation; otherwise N is 0.
  - V: No change
  - T: No change
  - **B**: No change
  - I: No change
  - **D**: No change
  - **Z**: Z is 1 when the operation result is 0; otherwise Z is 0.
  - **C**: C is 1 when the subtracted result is equal to or greater than 0; otherwise C is 0.

Addressing mode	Statement	Machine codes	Byte number	Cycle number
Immediate	∆CPY∆#\$nn	C016, nn16	2	2
Zero page	∆CPY∆\$zz	C416, ZZ16	2	3
Absolute	∆CPY∆\$hhll	CC16, II16, hh16	3	4

## DEC

### **DEC**REMENT BY ONE

**Operation :** (A)  $\leftarrow$  (A) - 1, or (M)  $\leftarrow$  (M) - 1

Function : This instruction subtracts 1 from the contents of A or M.

Status flag: N: N is 1 when bit 7 is 1 after the addition; otherwise N is 0.

- V: No change
- T: No change
- B: No change
- I: No change
- **D**: No change
- **Z**: Z is 1 when the operation result is 0; otherwise Z is 0.

DEC

C: No change

Addressing mode	Statement	Machine codes	Byte number	Cycle number
Accumulator	ΔDECΔΑ	1A16	1	2
Zero page	∆DEC∆\$zz	C616, ZZ16	2	5
Zero page X	∆DEC∆\$zz,X	D616, ZZ16	2	6
Absolute	∆DEC∆\$hhll	CE16, II16, hh16	3	6
Absolute X	∆DEC∆\$hhll,X	DE16, II16, hh16	3	7

RENESAS

# DEX DECREMENT INDEX REGISTER X BY ONE

**Operation** :  $(X) \leftarrow (X) - 1$ 

Function : This instruction subtracts one from the current contents of X.

- V: No change
- T: No change
- B: No change
- I: No change
- **D**: No change
- **Z**: Z is 1 when the operation result is 0; otherwise Z is 0.
- C: No change

Addressing mode	Statement	Machine codes	Byte number	Cycle number
Implied	ΔDEX	CA16	1	2

# DET DECREMENT INDEX REGISTER Y BY ONE

**Operation** :  $(Y) \leftarrow (Y) - 1$ 

Function : This instruction subtracts one from the current contents of Y.

- V: No change
- T: No change
- B: No change
- I: No change
- **D**: No change
- **Z**: Z is 1 when the operation result is 0; otherwise Z is 0.
- C: No change

Addressing mode	Statement	Machine codes	Byte number	Cycle number
Implied	ΔDEY	8816	1	2



### **DIV**IDE MEMORY BY ACCUMULATOR

DIV

Function :Divides the 16-bit data in M(zz+(X)) (low-order byte) and M(zz+(X)+1) (high-order byte) by the contents of A. The quotient is stored in A and the one's complement of the remainder is pushed onto the stack.



Status flag :No change

Addressing mode	Statement	Machine codes	Byte number	Cycle number
Zero page X	ΔDIVΔ\$zz,X	E216, zz16	2	16

- Notes 1: The quotient's overflow and zero division can not be detected. Check the quotient's overflow and zero division by software before DIV instruction is executed. This instruction changes the Stack Pointer and the contents of the Accumulator.
  - 2: The DIV instruction can not be used for some products.
  - 3: The DIV instruction is not affected by T and D flags.

EOR EXCLUSIVE OR MEMORY WITH ACCUMULATOR

- **Operation**: When (T) = 0,  $(A) \leftarrow (A) \forall (M)$ (T) = 1,  $(M(X)) \leftarrow (M(X)) \forall (M)$
- Function : When T = 0, this instruction transfers the contents of the M and A to the ALU which performs a bit-wise Exclusive OR, and stores the result in A.

When T = 1, the contents of M(X) and M are transferred to the ALU, which performs a bit-wise Exclusive OR and stores the results in M(X). The contents of A remain unchanged, but status flags are changed.

M(X) represents the contents of memory where is indicated by X.

- Status flag: N: N is 1 when bit 7 is 1 after the operation; otherwise N is 0.
  - V: No change
  - T: No change
  - B: No change
  - I: No change
  - **D**: No change
  - **Z**: Z is 1 when the operation result is 0; otherwise Z is 0.
  - C: No change

Addressing mode	Statement	Machine codes	Byte number	Cycle number
Immediate	∆EOR∆#\$nn	4916, nn16	2	2
Zero page	∆EOR∆\$zz	4516, zz16	2	3
Zero page X	∆EOR∆\$zz,X	5516, ZZ16	2	4
Absolute	∆EOR∆\$hhll	4D16, ll16, hh16	3	4
Absolute X	∆EOR∆\$hhll,X	5D16, ll16, hh16	3	5
Absolute Y	∆EOR∆\$hhll,Y	5916, ll16, hh16	3	5
(Indirect X)	∆EOR∆(\$zz,X)	4116, zz16	2	6
(Indirect Y)	∆EOR∆(\$zz),Y	5116, ZZ16	2	6

Note: When T=1, add 3 to the cycle number.

## INC

Function : This instruction adds one to the contents of A or M.

- V: No change
- T: No change
- B: No change
- I: No change
- **D**: No change
- **Z**: Z is 1 when the operation result is 0; otherwise Z is 0.
- C: No change

Addressing mode	Statement	Machine codes	Byte number	Cycle number
Accumulator	ΔΙΝCΔΑ	3A16	1	2
Zero page	∆INC∆\$zz	E616, ZZ16	2	5
Zero page X	∆INC∆\$zz,X	F616, ZZ16	2	6
Absolute	∆INC∆\$hhll	EE16, II16, hh16	3	6
Absolute X	∆INC∆\$hhll,X	FE16, II16, hh16	3	7

**Operation** :  $(X) \leftarrow (X) + 1$ 

Function : This instruction adds one to the contents of X.

- $\boldsymbol{V}$  : No change
- T: No change
- B: No change
- I: No change
- **D**: No change
- **Z**: Z is 1 when the operation result is 0; otherwise Z is 0.
- C: No change

Addressing mode	Statement	Machine codes	Byte number	Cycle number
Implied	ΔΙΝΧ	E816	1	2

**Operation** :  $(Y) \leftarrow (Y) + 1$ 

Function : This instruction adds one to the contents of Y.

- V: No change
- T: No change
- B: No change
- I: No change
- **D**: No change
- **Z**: Z is 1 when the operation result is 0; otherwise Z is 0.
- C: No change

Addressing mode	Statement	Machine codes	Byte number	Cycle number
Implied	ΔΙΝΥ	C816	1	2
function : This instruction jumps to the address designated by the following three addressing modes: Absolute Indirect Absolute Zero Page Indirect Absolute

Status flag: No change

Addressing mode	Statement	Machine codes	Byte number	Cycle number
Absolute	∆JMP∆\$hhll	4C16,II16,hh16	3	3
Indirect Absolute	$\Delta$ JMP $\Delta$ (\$hhll)	6C16,II16,hh16	3	5
Zero Page Indirect	∆JMP∆(\$zz)	B216,ZZ16	2	4

Note: The page's last address (address XXFF16) cannot be specified for the indirect designation address; in other words, JMP (\$XXFF) cannot be executed.

## JSR

 $\begin{array}{l} \textbf{Operation} : (M(S)) \leftarrow (PCH) \\ (S) \leftarrow (S) - 1 \\ (M(S)) \leftarrow (PCL) \\ (S) \leftarrow (S) - 1 \\ \text{After the above operations, if the addressing mode is} \\ (a) Absolute, then \\ (PC) \leftarrow hhll \\ (b) Special page, then \\ (PCL) \leftarrow II \\ (PCH) \leftarrow FF_{16} \\ (c) Zero page Indirect, then \\ (PCL) \leftarrow (zz) \\ (PCH) \leftarrow (zz+1) \end{array}$ 

Function : This instruction stores the contents of the PC in the stack, then jumps to the address designated by the following addressing modes: Absolute Special Page Zero Page Indirect Absolute

Status flag: No change

Addressing mode	Statement	Machine codes	Byte number	Cycle number
Absolute	∆JSR∆\$hhll	2016, II16, hh16	3	6
Special page	∆JSR∆\\$hhll (Note)	2216, II16	2	5
Zero page Indirect	$\Delta$ JSR $\Delta$ (\$zz)	0216, ZZ16	2	7

(Note) "\" (5C16 of the ASCII code) denotes special page. hh16 must be FF16 in the special page addressing mode.

# LDA LOAD ACCUMULATOR WITH MEMORY LDA

Operation : When (T) = 0,  $(A) \leftarrow (M)$ (T) = 1,  $(M(X)) \leftarrow (M)$ 

Function : When T = 0, this instruction transfers the contents of M to A. When T = 1, this instruction transfers the contents of M to (M(X)). The contents of A remain unchanged, but status flags are changed. M(X) represents the contents of memory where is indicated by

M(X) represents the contents of memory where is indicated by X.

- Status flag: N: N is 1 when bit 7 is 1 after the operation; otherwise N is 0.
  - V: No change
  - T: No change
  - B: No change
  - I: No change
  - **D**: No change
  - **Z**: Z is 1 when the operation result is 0; otherwise Z is 0.
  - C: No change

Addressing mode	Statement	Machine codes	Byte number	Cycle number
Immediate	∆LDA∆#\$nn	A916, nn16	2	2
Zero page	∆LDA∆\$zz	A516, zz16	2	3
Zero page X	ΔLDAΔ\$zz,X	B516, ZZ16	2	4
Absolute	∆LDA∆\$hhll	AD16, II16, hh16	3	4
Absolute X	∆LDA∆\$hhll,X	BD16, II16, hh16	3	5
Absolute Y	∆LDA∆\$hhll,Y	B916, II16, hh16	3	5
(Indirect X)	ΔLDAΔ(\$zz,X)	A116, zz16	2	6
(Indirect Y)	ΔLDAΔ(\$zz),Υ	B116, zz16	2	6

Note: When T = 1, add 2 to the cycle number.

RENESAS

# LDAD IMMEDIATE DATA TO MEMORY LDAD

**Operation** : (M)  $\leftarrow$  nn

Function : This instruction loads the immediate value in M.

Status flag : No change

Addressing mode	Statement	Machine codes	Byte number	Cycle number
Zero page	∆LDM∆#\$nn,\$zz	3C16, nn16, zz16	3	4

# $LDX_{\text{LOAD INDEX REGISTER X FROM MEMORY}} LDX$

**Operation** :  $(X) \leftarrow (M)$ 

Function : This instruction loads the contents of M in X.

Status flag: N: N is 1 when bit 7 is 1 after the operation; otherwise N is 0.

- V: No change
- T: No change
- **B**: No change
- I: No change
- **D**: No change
- **Z**: Z is 1 when the operation result is 0; otherwise Z is 0.
- C: No change

Addressing mode	Statement	Machine codes	Byte number	Cycle number
Immediate	∆LDX∆#\$nn	A216, nn16	2	2
Zero page	ΔLDXΔ\$zz	A616, ZZ16	2	3
Zero page Y	ΔLDXΔ\$zz,Y	<b>B6</b> 16, <b>ZZ</b> 16	2	4
Absolute	ΔLDXΔ\$hhll	AE16, II16, hh16	3	4
Absolute Y	∆LDX∆\$hhll,Y	BE16, II16, hh16	3	5

# LOAD INDEX REGISTER Y FROM MEMORY

**Operation** :  $(Y) \leftarrow (M)$ 

Function : This instruction loads the contents of M in Y.

Status flag: N: N is 1 when bit 7 is 1 after the operation; otherwise N is 0.

- V: No change
- T: No change
- B: No change
- I: No change
- **D**: No change
- **Z**: Z is 1 when the operation result is 0; otherwise Z is 0.

C: No change

Addressing mode	Statement	Machine codes	Byte number	Cycle number
Immediate	∆LDY∆#\$nn	A016, nn16	2	2
Zero page	ΔLDYΔ\$zz	A416, zz16	2	3
Zero page X	ΔLDYΔ\$zz,X	B416, ZZ16	2	4
Absolute	∆LDY∆\$hhll	AC16, II16, hh16	3	4
Absolute X	∆LDY∆\$hhll,X	BC16, II16, hh16	3	5

LSR	Logical Shift Right	R
<b>Operation</b> :	$0 \rightarrow b7$ $b0 \rightarrow C$	
Function :	This instruction shifts either A or M one bit to the right s that bit 7 of the result always is set to 0, and the bit stored in C.	such 0 is
Status flag:	N: 0	

- V: No change
- T: No change
- B: No change
- I: No change
- D: No change
- **Z**: Z is 1 when the operation result is 0; otherwise Z is 0.
- **C**: C is 1 when the bit 0 of either the A or the M before the operation is 1; otherwise C is 0.

Addressing mode	Statement	Machine codes	Byte number	Cycle number
Accumulator	ΔLSRΔA	4A16	1	2
Zero page	∆LSR∆\$zz	4616, zz16	2	5
Zero page X	∆LSR∆\$zz,X	5616, ZZ16	2	6
Absolute	∆LSR∆\$hhll	4E16, II16, hh16	3	6
Absolute X	∆LSR∆\$hhll,X	5E16, II16, hh16	3	7

# MULTIPLY ACCUMULATOR AND MEMORY MULTIPLY

**Function :** Multiplies Accumulator with the memory specified by the Zero Page X addressing mode and stores the high-order byte of the result on the Stack and the low-order byte in A.



Status flag : No change

Addressing mode	Statement	Machine codes	Byte number	Cycle number
Zero page X	ΔMULΔ\$zz,X	6216, ZZ16	2	15

Notes 1: This instruction changes the contents of S and A.

2: The MUL instruction cannot be used for some products.

3: The MUL instruction is not affected by T and D flags.

#### NO OPERATION

**Operation** : (PC)  $\leftarrow$  (PC) + 1

Function : This instruction adds one to the PC but does no other operation.

Status flag : No change

Addressing mode	Statement	Machine codes	Byte number	Cycle Number
Implied	ΔΝΟΡ	EA16	1	2

### ORA

## ORA

#### **OR** MEMORY WITH **A**CCUMULATOR

- Operation : When (T) = 0,  $(A) \leftarrow (A) \lor (M)$ (T) = 1,  $(M(X)) \leftarrow (M(X)) \lor (M)$
- Function : When T = 0, this instruction transfers the contents of A and M to the ALU which performs a bit-wise "OR", and stores the result in A. When T = 1 this instruction transfers the contents of M(X) and

When T = 1, this instruction transfers the contents of M(X) and the M to the ALU which performs a bit-wise OR, and stores the result in M(X). The contents of A remain unchanged, but status flags are changed.

M(X) represents the contents of memory where is indicated by X.

### Status flag: N: N is "1" when bit 7 is 1 after the operation; otherwise N is 0.

- V: No change
- T: No change
- **B**: No change
- I: No change
- **D**: No change
- **Z**: Z is 1 when the execution result is 0; otherwise Z is 0.
- C: No change

Addressing mode	Statement	Machine codes	Byte number	Cycle number
Immediate	∆ORA∆#\$nn	0916, nn16	2	2
Zero page	∆ORA∆\$zz	0516, ZZ16	2	3
Zero page X	∆ORA∆\$zz,X	1516, zz16	2	4
Absolute	∆ORA∆\$hhll	0D16, II16, hh16	3	4
Absolute X	∆ORA∆\$hhll,X	1D16, II16, hh16	3	5
Absolute Y	∆ORA∆\$hhll,Y	1916, II16, hh16	3	5
(Indirect X)	∆ORA∆(\$zz,X)	0116, zz16	2	6
(Indirect Y)	∆ORA∆(\$zz),Y	1116, ZZ16	2	6

Note: When T=1, add 3 to the cycle number.



#### 

Function : This instruction pushes the contents of A to the memory location designated by S, and decrements the contents of S by one.

Status flag : No change

Addressing mode	Statement	Machine codes	Byte number	Cycle number
Implied	ΔPHA	4816	1	3



**Function** : This instruction pushes the contents of PS to the memory location designated by S and decrements the contents of S by one.

Status flag: No change

Addressing mode	Statement	Machine codes	Byte number	Cycle number
Implied	ΔPHP	0816	1	3



#### PULL ACCUMULATOR FROM STACK

 $\begin{array}{l} \textbf{Operation} : (S) \leftarrow (S) + 1 \\ (A) \leftarrow (M(S)) \end{array}$ 

- **Function** : This instruction increments S by one and stores the contents of the memory designated by S in A.
- Status flag: N:N is 1 when bit 7 is 1 after the operation ; otherwise N is 0.
  - V: No change
  - T: No change
  - **B**: No change
  - I: No change
  - **D**: No change
  - **Z**: Z is 1 when the operation result is 0; otherwise Z is 0.
  - C: No change

Addressing mode	Statement	Machine codes	Byte number	Cycle number
Implied	ΔPLA	<b>68</b> 16	1	4

Note: A NOP instruction should be executed after every PLP instruction.



### $\begin{array}{l} \textbf{Operation} : (S) \leftarrow (S) + 1 \\ (PS) \leftarrow (M(S)) \end{array}$

**Function** : This instruction increments S by one and stores the contents of the memory location designated by S in PS.

 $Status\ flag$  : Value returns to the original one that was pushed in the stack.

Addressing mode	Statement	Machine codes	Byte number	Cycle number
Implied	ΔPLP	2816	1	4

Note: A NOP instruction should be executed after every PLP instruction.

### ROL

ROTATE ONE BIT LEFT

ROL

**Operation** :



**Function :** This instruction shifts either A or M one bit left through C. C is stored in bit 0 and bit 7 is stored in C.

Status flag: N: N is 1 when bit 6 is 1 before the operation; otherwise N is 0.

- V: No change
- T: No change
- B: No change
- I: No change
- **D**: No change
- **Z**: Z is 1 when the operation result is 0; otherwise Z is 0.

**C**: C is 1 when bit 7 is 1 before the operation; otherwise C is

0.

Addressing mode	Statement	Machine codes	Byte number	Cycle number
Accumulator	ΔROLΔΑ	2A16	1	2
Zero page	∆ROL∆\$zz	2616, ZZ16	2	5
Zero page X	∆ROL∆\$zz,X	3616, zz16	2	6
Absolute	∆ROL∆\$hhll	2E16, II16, hh16	3	6
Absolute X	∆ROL∆\$hhll,X	3E16, II16, hh16	3	7

RENESAS



Addressing mode	Statement	Machine codes	Byte number	Cycle number
Accumulator	ΔRORΔA	6A16	1	2
Zero page	∆ROR∆\$zz	6616, ZZ16	2	5
Zero page X	∆ROR∆\$zz,X	7616, ZZ16	2	6
Absolute	∆ROR∆\$hhll	6E16, II16, hh16	3	6
Absolute X	∆ROR∆\$hhll,X	7E16, II16, hh16	3	7



#### ROTATE RIGHT OF FOUR BITS

**Operation** :



Function : This instruction rotates 4 bits of the M content to the right.

Status flag : No change

Addressing mode	Statement	Machine codes	Byte number	Cycle number
Zero page	∆RRF∆\$zz	8216, ZZ16	2	8

## RTI

- $\begin{array}{l} \textbf{Operation}: (S) \leftarrow (S) + 1 \\ (PS) \leftarrow (M(S)) \\ (S) \leftarrow (S) + 1 \\ (PCL) \leftarrow (M(S)) \\ (S) \leftarrow (S) + 1 \\ (PCH) \leftarrow (M(S)) \end{array}$
- **Function** : This instruction increments S by one, and stores the contents of the memory location designated by S in PS. S is again incremented by one and stores the contents of the memory location designated by S in PCL. S is again incremented by one and stores the contents of memory location designated by S in PCH.

Status flag: Value returns to the original one that was pushed in the stack.

Addressing mode	Statement	Machine codes	Byte number	Cycle number
Implied	ΔRTI	4016	1	6

### RTS

 $\begin{array}{l} \textbf{Operation}:\ (S) \leftarrow (S) + 1 \\ (PCL) \leftarrow (M(S)) \\ (S) \leftarrow (S) + 1 \\ (PCH) \leftarrow (M(S)) \\ (PC) \leftarrow (PC) + 1 \end{array}$ 

**Function :** This instruction increments S by one and stores the contents of the memory location designated by S in PCL. S is again incremented by one and the contents of the memory location is stored in PCH. PC is incremented by 1.

Status flag: No change

Addressing mode	Statement	Machine codes	Byte number	Cycle number
Implied	∆RTS	6016	1	6

#### SUBTRACT WITH CARRY

Function : When T = 0, this instruction subtracts the value of M and the complement of C from A, and stores the results in A and C. When T = 1, the instruction subtracts the contents of M and the complement of C from the contents of M(X), and stores the results in M(X) and C. A remain unchanged, but status flag are changed.

M(X) represents the contents of memory where is indicated by X.

**SBC** 

### Status flag: N: N is 1 when bit 7 is 1 after the operation; otherwise N is 0.

- V: V is 1 when the operation result exceeds +127 or |-128|; otherwise V is 0.
- T: No change
- B: No change
- I: No change
- **D**: No change
- **Z**: Z is 1 when the operation result is 0; otherwise Z is 0.
- **C**: C is 1 when the subtracted result is equal to or greater than 0; otherwise C is 0.

Addressing mode	Statement	Machine codes	Byte number	Cycle number
Immediate	∆SBC∆#\$nn	E916, nn16	2	2
Zero page	∆SBC∆\$zz	E516, zz16	2	3
Zero page X	∆SBC∆\$zz,X	F516, zz16	2	4
Absolute	∆SBC∆\$hhll	ED16, ll16, hh16	3	4
Absolute X	∆SBC∆\$hhll,X	FD16, II16, hh16	3	5
Absolute Y	∆SBC∆\$hhll,Y	F916, II16, hh16	3	5
(Indirect X)	$\Delta$ SBC $\Delta$ (\$zz,X)	E <b>1</b> 16, zz16	2	6
(Indirect Y)	∆SBC∆(\$zz),Y	F116, zz16	2	6

Notes 1: When T=1, add 3 to the cycle number.

2: When SBC instruction is executed in decimal operation mode (D = 1), execute at least one instruction after the SBC instruction before executing a SEC, CLC, or CLD instruction.

In decimal operation mode, the N, V, Z flags are invalid.

### **SEB**

Function : This instruction sets the designated bit i of A or M.

Status flag: No change

Addressing mode	Statement	Machine codes	Byte number	Cycle number
Accumulator bit	∆SEB∆i,A	(20i+B)16	1	2
Zero page bit	∆SEB∆i,\$zz	(20i+F)16, zz16	2	5

### SEC

**Operation** :  $(C) \leftarrow 1$ 

Function : This instruction sets C.

Status flag: N: No change V: No change T: No change B: No change I: No change

- D: No change
- Z: No change
- **C**: 1

Addressing mode	Statement	Machine code	Byte number	Cycle number
Implied	ΔSEC	3816	1	2

## SED

**Operation** :  $(D) \leftarrow 1$ 

Function : This instruction set D.

Status flag:N : No changeV : No changeT : No changeB : No changeI : No changeD : 1Z : No changeC : No change

Addressing mode	Statement	Machine codes	Byte number	Cycle number
Implied	ΔSED	F816	1	2

### SEI

**Operation** : (I)  $\leftarrow$  1

Function : This instruction sets I.

Status flag: N : No change
V : No change
T : No change
B : No change
I : 1
D : No change
Z : No change
C : No change

Addressing mode	Statement	Machine codes	Byte number	Cycle number
Implied	∆SEI	<b>78</b> 16	1	2

## SET

**Operation** :  $(T) \leftarrow 1$ 

Function : This instruction sets T.

Status	flag:	N :	No	change
		<b>V</b> :	No	change
		Т:	1	
		В:	No	change
		1:	No	change
		D :	No	change
		Ζ:	No	change
		<b>C</b> :	No	change

Addressing mode	Statement	Machine codes	Byte number	Cycle number
Implied	∆SET	3216	1	2

**Operation** :  $(M) \leftarrow (A)$ 

**Function :** This instruction stores the contents of A in M. The contents of A does not change.

Status flag: No change

Addressing mode	Statement	Machine codes	Byte number	Cycle number
Zero page	∆STA∆\$zz	8516, ZZ16	2	4
Zero page X	∆STA∆\$zz,X	9516, ZZ16	2	5
Absolute	∆STA∆\$hhll	8D16, ll16, hh16	3	5
Absolute X	∆STA∆\$hhll,X	9D16, ll16, hh16	3	6
Absolute Y	∆STA∆\$hhll,Y	9916, ll16, hh16	3	6
(Indirect X)	∆STA∆(\$zz,X)	8116, ZZ16	2	7
(Indirect Y)	∆STA∆(\$zz),Y	9116, ZZ16	2	7

**Operation :** CPU  $\leftarrow$  Stand-by state (Oscillation stopped)

**Function :** This instruction resets the oscillation control F/F and the oscillation stops. Reset or interrupt input is needed to wake up from this mode.

Status flag: No change

Addressing mode	Statement	Machine codes	Byte number	Cycle number
Implied	ΔSTP	4216	1	2

Note: If the STP instruction is disabled the cycle number will be 2 (same in operation as NOP). However, disabling this instruction is an optional feature; therefore, consult the specifications for the particular chip in question.

**Operation** :  $(M) \leftarrow (X)$ 

**Function :** This instruction stores the contents of X in M. The contents of X does not change.

Status flag: No change

Addressing mode	Statement	Machine codes	Byte number	Cycle number
Zero page	∆STX∆\$zz	8616, ZZ16	2	4
Zero page Y	∆STX∆\$zz,Y	9616, zz16	2	5
Absolute	∆STX∆\$hhll	8E16, II16, hh16	3	5

#### **Operation** : $(M) \leftarrow (Y)$

**Function :** This instruction stores the contents of Y in M. The contents of Y does not change.

Status flag: No change

Addressing mode	Statement	Machine codes	Byte number	Cycle number
Zero page	ΔSTYΔ\$zz	8416, ZZ16	2	4
Zero page X	∆STY∆\$zz,X	9416, zz16	2	5
Absolute	∆STY∆\$hhll	8C16, II16, hh16	3	5

**Operation** :  $(X) \leftarrow (A)$ 

**Function :** This instruction stores the contents of A in X. The contents of A does not change.

### Status flag: N: N is 1 when bit 7 is 1 after the operation; otherwise N is 0.

- V: No change
- T: No change
- B: No change
- I: No change
- **D**: No change
- **Z**: Z is 1 when the operation result is 0; otherwise Z is 0.
- C: No change

Addressing mode	Statement	Machine codes	Byte number	Cycle number
Implied	ΔΤΑΧ	AA16	1	2

# TAY TRANSFER ACCUMULATOR TO INDEX REGISTER Y

**Operation** :  $(Y) \leftarrow (A)$ 

**Function :** This instruction stores the contents of A in Y. The contents of A does not change.

Status flag: N: N is 1 when bit 7 is 1 after the operation; otherwise N is 0.

- V: No change
- T: No change
- B: No change
- I: No change
- **D**: No change
- **Z**: Z is 1 when the operation result is 0; otherwise Z is 0.
- **C**: No change

Addressing mode	Statement	Machine codes	Byte number	Cycle number
Implied	ΔΤΑΥ	A816	1	2

### TST

**Operation** : (M) = 0?

Function : This instruction tests whether the contents of M are "0" or not and modifies the N and Z.

Status flag: N: N is 1 when bit 7 of M is 1; otherwise N is 0.

- V: No change
- T: No change
- B: No change
- I: No change
- **D**: No change
- **Z**: Z is 1 when the M content is 0; otherwise Z is 0.

C: No change

Addressing mode	Statement	Machine codes	Byte number	Cycle number
Zero page	ΔTSTΔ\$zz	6416, ZZ16	2	3

# $TSX_{\text{TRANSFER STACK POINTER TO INDEX REGISTER X}}TSX$

**Operation** :  $(X) \leftarrow (S)$ 

Function : This instruction transfers the contents of S in X.

Status flag: N: N is 1 when bit 7 is 1 after the operation; otherwise N is 0.

- V: No change
- T: No change
- B: No change
- I: No change
- **D**: No change
- **Z**: Z is 1 when the operation result is 0; otherwise Z is 0.

C: No change

Addressing mode	Statement	Machine codes	Byte number	Cycle number
Implied	ΔTSX	BA16	1	2

RENESAS

#### TXA TRANSFER INDEX REGISTER X TO ACCUMULATOR

**Operation** :  $(A) \leftarrow (X)$ 

Function : This instruction stores the contents of X in A.

Status flag: N: N is 1 when bit 7 is 1 after the operation; otherwise N is 0.

- V: No change
- T: No change
- B: No change
- I: No change
- **D:** No change
- **Z**: Z is 1 when the operation result is 0; otherwise Z is 0.

C: No change

Addressing mode	Statement	Machine codes	Byte number	Cycle number
Implied	ΔΤΧΑ	8A16	1	2

### TXS TRANSFER INDEX REGISTER X TO STACK POINTER TXS

**Operation** :  $(S) \leftarrow (X)$ 

Function : This instruction stores the contents of X in S.

Status flag No change

Addressing mode	Statement	Machine codes	Byte number	Cycle number
Implied	ΔTXS	9A16	1	2

#### TYA TRANSFER INDEX REGISTER Y TO ACCUMULATOR

**Operation** :  $(A) \leftarrow (Y)$ 

Function : This instruction stores the contents of Y in A.

Status flag: N: N is 1 when bit 7 is 1 after the operation; otherwise N is 0.

- V: No change
- T: No change
- B: No change
- I: No change
- **D:** No change
- **Z**: Z is 1 when the operation result is 0; otherwise Z is 0.
- C: No change

Addressing mode	Statement	Machine codes	Byte number	Cycle number
Implied	ΔΤΥΑ	9816	1	2
## **Operation :** CPU $\leftarrow$ Wait state

**Function :** The WIT instruction stops the internal clock but the oscillation of the oscillation circuit is not stopped. Reset or interrupt input is needed to wake up from this mode.

WAIT

Status flag: No change

Addressing mode	Statement	Machine codes	Byte number	Cycle number
Implied	ΔWIT	C216	1	2

## **INSTRUCTIONS**

## Instructions Related to Interrupt Processing and Subroutine Processing

### 3.4 Instructions Related to Interrupt Handling and Subroutine Processing

#### 3.4.1 Instructions Related to Interrupt Handling

When an interrupt is accepted, the contents of the processor status register are pushed onto the memory location indicated by the stack pointer. <u>There is therefore no need to execute the PHP instruction.</u>

If it is necessary to save the contents of the accumulator, the PHA instruction should be executed within an interrupt routine (before any instruction that manipulates the accumulator). Whenever a stack operation instruction such as PHA is executed within an interrupt routine, make sure that instructions such as PLA that affect the stack operation instruction are also executed within the same interrupt routine.

Execute the RTI instruction to return from the interrupt routine.

#### 3.4.2 Instructions Related to Interrupt Control

The factors that control an interrupt are the interrupt disable flag (I) as well as the interrupt enable bit and request bit corresponding to the interrupt source. (This does not apply to software interrupts triggered by the BRK instruction.)

### (1) Disabling Interrupts

An interrupt may be disabled by setting the interrupt disable flag (I) to "1" using the SEI instruction or by using an instruction such as LDM or CLB (a variety of other instructions can be used as well) to clear the interrupt enable bit to "0".

#### (2) Enabling Interrupts

An interrupt may be enabled by setting the interrupt enable bit to "1" using an instruction such as LDM or SEB, and by using the CLI instruction to clear the interrupt disable flag (I) to "0".

### (3) Clearing Interrupt Requests

When an interrupt is generated, the interrupt request bit corresponding to the interrupt source is set to "1" automatically. The interrupt request bit is cleared to "0" when the interrupt is accepted. Therefore, there is no need to clear the interrupt request bit (within an interrupt routine) by means of a user program.

If interrupt generation occurs while an interrupt is disabled, the interrupt request bit is set to "1". If, under this condition, the interrupt is subsequently enabled (the interrupt disable flag (I) is cleared to "0" and the interrupt enable bit is set to "1"), the interrupt is accepted. To prevent an interrupt from being accepted in such a case, use an instruction such as LDM or CLB to clear the interrupt request bit to "0" before enabling the interrupt. In such cases, the following point should be considered.

•While the interrupt disable flag (I) is "0", if the interrupt request bit is cleared to "0" and the interrupt enable bit is cleared to "0" at the same time using an instruction such as LDM, the interrupt will actually be enabled before the request bit is cleared to "0", <u>causing the interrupt to be accepted.</u>

To prevent this, use an instruction such as CLB to <u>clear the request bit to "0" first, then</u> enable the interrupt.

## **INSTRUCTIONS**

## Instructions Related to Interrupt Processing and Subroutine Processing

### (4) Interrupt Control within Interrupt Routines

After an interrupt is accepted and execution of the interrupt routine begins, the interrupt disable flag (I) is set to "1" automatically to prevent multiple interrupts. <u>To enable multiple interrupts</u>, use the CLI instruction within the interrupt routine to clear the interrupt disable flag (I) to "0".

### 3.4.3 Instructions Related to Subroutine Processing

Normally, the JSR instruction is used to jump to a subroutine. When this instruction is executed, the current program counter values, first PCH then PCL, are pushed onto the stack automatically and the stack pointer is moved accordingly. However, in contrast to interrupt handling, the contents of the processor status register are not saved automatically when a subroutine is called. If it is necessary to save the contents of the processor status register, execute the PHP instruction. Executing the JSR instruction does not alter the content of the processor status register. Therefore, saving the contents of the processor status register using the PHP instruction may be performed either immediately before the JSR instruction or immediately after it (at the beginning of the subroutine). However, if such a stack operation instruction is executed within a subroutine, do not fail to perform the opposite operation before returning from (that is, within) the subroutine.

<u>Execute the RTS instruction to return from a subroutine.</u> When this instruction is executed, the return address saved by the JSR instruction is returned to the program counter automatically. Likewise in contrast to interrupt handling, the contents of the processor status register are not restored. If the PHP or PHA instruction is used within a subroutine to store the contents of the processor status register or accumulator, do not fail to perform the opposite stack operation, using the PLP or PLA instruction, before returning from (that is, within) the subroutine.

Figure 3.4.1 shows pushing and pulling values onto and from the stack during interrupt handling and subroutine processing. Table 3.4.1 shows instructions for storing and retrieving values in the accumulator and processor status register.

# **INSTRUCTIONS**





Fig.3.4.1 Pushing and pulling values onto and from the stack

Table 3	.4.1	Instructions	for	storing	and	retrieving	values	in the	accumulator	or	processor	status	register
---------	------	--------------	-----	---------	-----	------------	--------	--------	-------------	----	-----------	--------	----------

	Instruction to push onto Stack	Instruction to pull from Stack
Accumulator	PHA	PLA
Processor status register	PHP	PLP

## 4. NOTES ON USE

The information below applies to the entire 740 Family. Please refer to it in conjunction with the usage notes of each specific product model.

#### 4.1 Notes on input and output ports

#### 4.1.1 Notes in standby state

In standby state<sup>\*1</sup>, do not make pin levels "undefined" when I/O ports are set to input mode. In addition, the same note is necessary even when N-channel open-drain I/O ports are set to output mode.

Pull-up (connect the port to  $V_{\mbox{\scriptsize Cc}})$  or pull-down (connect the port to  $V_{\mbox{\scriptsize Ss}})$  these ports through a resistor.

When determining a resistance value, note the following points:

- External circuit
- Variation of output levels during the ordinary operation
- ●Reason

An transistor becomes an OFF state when an I/O port is set as input mode by the direction register, so that the port enter a high-impedance state. At this time, the potential which is input to the input buffer in a microcomputer is unstable in the state that input levels are "undefined". This may cause power source current. Even when an I/O port of N-channel open-drain is set as output mode by the direction register, if the contents of the port latch is "1", the same phenomenon as that of an input port will occur.

\*1 standby state: Stop mode by executing STP instruction Wait mode by executing WIT instruction

### 4.1.2 Modifying output data with bit managing instruction

When the port latch of an I/O port is modified with the bit managing instruction<sup>\*2</sup>, the value of the unspecified bit may be changed.

#### ●Reason

I/O ports are set to input or output mode in bit units. Reading from a port register or writing to it involves the following operations.

• Port in input mode

Read: Read the pin level.

Write: Write to the port latch.

• Port in output mode

Read: Read the port latch or read the output from the peripheral function (specifications differ depending on the port).

Write: Write to the port latch. (The port latch value is output from the pin.)

Since bit managing instructions<sup>\*1</sup> are read-modify-write instructions, <sup>\*2</sup> using such an instruction on a port register causes a read and write to be performed simultaneously on the bits other than the one specified by the instruction.

When an unspecified bit is in input mode, its pin level is read and that value is written to the port latch. If the previous value of the port latch differs from the pin level, the port latch value is changed.

If an unspecified bit is in output mode, the port latch is generally read. However, for some ports the peripheral function output is read, and the value is written to the port latch. In this case, if the previous value of the port latch differs from the peripheral function output, the port latch value is changed.

- \*1. Bit managing instructions: SEB and CLB instructions
- \*2. Read-modify-write instructions: Instructions that read memory in byte units, modify the value, and then write the result to the same location in memory in byte units

# NOTES ON USE

### 4.2 Termination of unused pins

At the termination of unused pins, perform wiring at the shortest possible distance (20 mm or less) from microcomputer pins. With regard to an effects on the system, thoroughly perform system evaluation on the user side.

### 4.2.1 Appropriate termination of unused pins

① Output-only pins:

Open.

2 Input-only pins:

Connect each pin via a 1 k $\Omega$  to 10 k $\Omega$  resistor (reference value) to V<sub>cc</sub> or V<sub>ss</sub>. If the port allows selection of an on-chip pull-up or pull-down resistor, the on-chip pull-up or pull-down resistor may be used.

In addition, pins (CNVss and INT pins, etc.) for which the operating mode is affected by the voltage level, select  $V_{cc}$  or  $V_{ss}$  after checking the mode.

③ I/O ports:

Set the I/O ports for the input mode and connect them to V<sub>cc</sub> or V<sub>ss</sub> through each resistor of 1 k $\Omega$  to 10 k $\Omega$  (reference value).

Ports that permit the selecting of a built-in pull-up/pull-down resistor can also use this resistor. Set the I/O ports for the output mode and open them at "L" or "H".

- When opening them in the output mode, the input mode of the initial status remains until the mode of the ports is switched over to the output mode by the program after reset. Thus, the potential at these pins is undefined and the power source current may increase in the input mode. With regard to an effects on the system, thoroughly perform system evaluation on the user side.
- Since the direction register setup may be changed because of a program runaway or noise, set direction registers by program periodically to increase the reliability of program.

④ The AVss pin when not using the A/D converter: When not using the A/D converter, handle a power source pin for the A/D converter, AVss and AVcc pins as follows:

• AVss: Connect to the Vss pin.

• AVcc: Connect to the Vcc pin.

## 4.2.2 Termination remarks

### ① I/O ports:

Do not open in the input mode.

●Reason

- The power source current may increase depending on the first-stage circuit.
- An effect due to noise may be easily produced as compared with proper termination ① and shown on the above.
- 2 I/O ports:

When setting for the input mode, do not connect to  $V_{\text{CC}}$  or  $V_{\text{SS}}$  directly.

Reason

If the direction register setup changes for the output mode because of a program runaway or noise, a short circuit may occur between a port and  $V_{cc}$  (or  $V_{ss}$ ).

③ I/O ports:

When setting for the input mode, do not connect multiple ports in a lump to  $V_{\text{CC}}$  or  $V_{\text{SS}}$  through a resistor.

Reason

If the direction register setup changes for the output mode because of a program runaway or noise, a short circuit may occur between ports.

### 4.3 Notes on interrupts

### 4.3.1 Setting for interrupt request bit and interrupt enable bit

To set an interrupt request bit and an interrupt enable bit for interrupts, execute as the following sequence:

- ① Clear an interrupt request bit to "0" (no interrupt request issued).
- ② Set an interrupt enable bit to "1" (interrupts enabled).
- ●Reason

If the above setting are performed simultaneously with one instruction, an unnecessary interrupt processing routine is executed. Because an interrupt enable bit is set to "1" (interrupts enabled) before an interrupt request bit is cleared to "0."

### 4.3.2 Switching of detection edge

If it is not necessary to generate interrupts synchronized with certain settings, such as setting the active edge for external interrupts or switching the interrupt source for a vector in cases where multiple interrupt sources are assigned to the same interrupt vector, use the following procedure to make the settings.



Fig. 4.3.1 Switching sequence of detection edge

### ●Reason

The interrupt request bit may be set to "1" in the following cases:

- When switching the active edge for external interrupts.
- When switching the interrupt source for a vector in cases where multiple interrupt sources are assigned to the same interrupt vector.

# NOTES ON USE

## 4.3.3 Distinction of interrupt request bit

When executing the BBC or BBS instruction to an interrupt request (request distinguish) bit of an interrupt request register (interrupt request distinguish register) immediately after this bit is set to "0", execute one or more instructions before executing the BBC or BBS instruction.



Fig. 4.3.2 Distinction sequence of interrupt request bit

## ●Reason

If the BBC or BBS instruction is executed immediately after an interrupt request (request distinguish) bit of an interrupt request register (interrupt request distinguish register) is cleared to "0," the value of the interrupt request (request distinguish) bit before being cleared to "0" is read.

### 4.4 Notes on programming

#### 4.4.1 Processor Status Register

#### (1) Initialization of Processor Status Register

Flags which affect program execution must be initialized after a reset. In particular, it is essential to initialize the T and D flags because they have an important effect on calculations.

#### ●Reason

After a reset, the contents of processor status register (PS) are undefined except for the I flag which is "1."



Fig. 4.4.1 Initialization of flags in Processor Status Register

### (2) How to reference Processor Status Register

To reference the contents of the processor status register (PS), execute the PHP instruction once then read the contents of (S + 1). If necessary, execute the PLP instruction to return the PS to its original status.

A NOP instruction should be executed after every PLP instruction.



Fig. 4.4.2 PLP instruction execution sequence



Fig. 4.4.3 Stack memory contents after PHP instruction execution

## 4.4.2 BRK instruction

### (1) Method detecting interrupt source

It can be detected that the BRK instruction interrupt event or the least priority interrupt event by referring the stored B flag state. Refer the stored B flag state in the interrupt routine, in this case.





## (2) Interrupt priority level

- At the following status,
- ① the interrupt request bit has set to "1."
- $\ensuremath{\textcircled{}^\circ}$  the interrupt enable bit has set to "1."
- 3 the interrupt disable flag (I) has set to "1."

If the BRK instruction is executed, the interrupt disable state is cancelled and it becomes in the interrupt enable state. So that the requested interrupts (the interrupts that corresponding to their request bits have set to "1") are accepted.

## 4.4.3 Decimal calculations

### (1) Execution of Decimal calculations

The ADC and SBC are the only instructions which will yield proper decimal results in decimal mode. To calculate in decimal notation, set the decimal mode flag (D) to "1" with the SED instruction. After executing the ADC or SBC instruction, execute another instruction before executing the SEC, CLC, or CLD instruction.

## (2) Status flags in decimal mode

When decimal mode is selected (D = 1), the values of three of the flags in the status register (the flags N, V, and Z) are invalid after a ADC or SBC instruction is executed. The carry flag (C) is set to "1" if a carry is generated as a result of the calculation, or is cleared to "0" if a borrow is generated. To determine whether a calculation has generated a carry, the C flag must be initialized to "0" before each calculation. To check for a borrow, the C flag must be initialized to "1" before each calculation.



Fig. 4.4.5 Status flags in decimal mode

## 4.4.4 JMP instruction

When using the JMP instruction in indirect addressing mode, do not specify the last address on a page as an indirect address.

## 4.4.5 Multiplication and division instructions

The index mode (T) and the decimal mode (D) flags do not affect the MUL and DIV instruction. The execution of these instructions does not change the contents of the processor status register.

## 4.4.6 Ports

The contents of the port direction registers cannot be read.

The following cannot be used:

- The data transfer instruction (LDA, etc.)
- The operation instruction when the index X mode flag (T) is "1"
- The addressing mode which uses the value of a direction register as an index
- The bit-test instruction (BBC or BBS, etc.) to a direction register
- The read-modify-write instruction (ROR, CLB, or SEB, etc.) to a direction register
- Use instructions such as LDM and STA, etc., to set the port direction registers.

## 4.4.7 Instruction execution time

The instruction execution time is obtained by multiplying the frequency of the internal clock  $\phi$  by the number of cycles needed to execute an instruction.

The number of cycles required to execute an instruction is shown in the list of machine instructions.

# APPENDIX 1 Instruction Cycles in each Addressing Mode

## **APPENDIX 1. Instruction Cycles in each Addressing Mode**

Clock  $\phi$  controls the system timing of 740 Family. The SYNC signal and the value of PC (Program Counter) are output in every instruction fetch cycle. The Op-Code is fetched during the next half-period of  $\phi$ . The instruction decoder of CPU decodes this Op-Code and determines the following how to execute the instruction. The instruction timings of all addressing modes are described on the following pages.

The  $\phi$ , SYNC, R/W (RD, WR), ADDR (ADDRL, ADDRH), and DATA signals in these figures indicate the status of the internal bus. These signals cannot be seen directly in single-chip mode, but they can be checked on products that support use of microprocessor mode.

The combination of these signals differs according to the microcomputer's type. The following table lists the valid signal for each product.

Туре	$\phi$	SYNC	R/W	RD	WR	ADDR	DATA	<b>ADDR</b> H	ADDRL/DATA
M507XX M509XX									
M374XX	0	0	0			0	0		
(Except M37451)									
M38XXX									
M375XX	$\bigcirc$	$\cap$		$\cap$	$\cap$	$\cap$	$\cap$		
M372XX	$\bigcirc$	Ŭ		Ŭ	Ŭ	Ŭ	Ŭ		
M371XX									
M37451	0	0	0	O (Note)	O (Note)	0	0		
M50734	0	0		0	0			0	0

Valid signal for each product

Note: Only 80-pin version.

: <b>ACLC</b>	∆SEC
∆CLD	$\Delta$ SED
∆CLI	∆SEI
∆CLT	∆SET
ACLV	ΔΤΑΧ
∆ <b>DEX</b>	ΔΤΑΥ
∆DEY	ATSX
ΔΙΝΧ	ΔΤΧΑ
ΔΙΝΥ	∆ <b>TXS</b>
ANOP	ΔΤΥΑ
: 1	
: <b>2</b>	
	: ΔCLC ΔCLD ΔCLI ΔCLT ΔCLV ΔDEX ΔDEY ΔINX ΔINY ΔNOP : 1 : 2

:

Timing





Notes 1 : Some products are "01" or content of SPS flag. 2 : Some products differ the address.

Instructions			
Byte length	۵₩۲ : 1		
Timing	:		
φ			
SYNC			
R/W			
RD			
WR			
ADDR	PC	PC+1	
DATA	Op-code	Invalid	
ADDRH	РСН	РСн	 X
ADDRL /DATA	PCL Op- code PCL+1 In- valid	PCL+1	

Retum from standby state is excuted by extemal interrupt. Retum from wait state is excuted by internal or external interrupt.



Note: Some products are "01" or content of SPS flag.



Note: Some products are "01" or content of SPS flag.



Note: Some products are "01" or content of SPS flag.



Note: Some products are "01" or content of SPS flag.

[T=0]

Instructions	:	ΔADC∆#\$nn ΔAND∆#\$nn ΔCMP∆#\$nn ΔCPX∆#\$nn ΔCPX∆#\$nn	(T=0) (T=0) (T=0)	
		ΔEORΔ#\$nn ΔLDAΔ#\$nn ΔLDXΔ#\$nn ΔLDXΔ#\$nn ΔLDYΔ#\$nn	(T=0) (T=0)	
		∆ORA∆#\$nn ∆SBC∆#\$nn	(T=0) (T=0)	
Byte length Cycle number	:	2 2		
Timing	:			
	ф			
				Г



PCL+1 DATA

/DATA

## ACCUMULATOR



# **ACCUMULATOR BIT RELATIVE**

Instructions	: △BBC∆i,A,\$hhll △BBS∆i A \$hhll
Byte length	: 2
(1) With no bi Cycle number	ranch : <b>4</b>
Timing	:
ф	
SYNC	
R/W	
RD	
WR	
ADDR	PC PC+1
DATA	Op-code Invalid
ADDRH	РСН РСН
ADDRL /DATA	PCL Op- wde PCL+1 In- valid PCL+1 In- valid PCL+1 In- valid PCL+1 Valid PCL+1 VAL+1 Valid PCL+1 Valid PCL+1 VAL+1 VAL+1 VAL+1 VAL+1 VAL+1 VAL+1 VA

# **ACCUMULATOR BIT RELATIVE**

Instructions	: △BBC△i,A,\$hhll △BBS△i A \$bbll
Byte length	: <b>2</b>
(2) With branch Cycle number	ר נייני <b>6</b>
Timing	:
ф	
SYNC	
R/W	
RD	
WR	
ADDR	PC PC+1 (PC+2)L ((PC+2)±RR)L (PC+2) H (PC+2) H
DATA	Op-code Invalid ±RR Invalid Inva
ADDRH	PCH PCH (PC+2)H (PC+2)H
ADDRL /DATA	PCL Op- code PCL+1 In- valid PCL+1 In- valid PCL+1 ±RR *1 *2 (*2
RR : Offset *1 : (PC+1) *2 : ((PC+2	address )L 2) ± RR)L

# **ACCUMULATOR BIT**

Instructions	: <b>ΔCLBΔi,A</b> ΔSEBΔi,A	
Byte length Cycle number	:1 :2	
Timing	:	
	φ	
	SYNC	
	R/W	
	RD	
	WR	
	ADDR	PC PC+1
	DATA	Op-code Invalid
	ADDRH	РСН РСН
	ADDRL /DATA	PCL Op- code PCL+1 In- valid

## **BIT RELATIVE**

Instructions : **\Delta BBC**\Delta i,\$zz,\$hhll ∆BBS∆i,\$zz,\$hhll Byte length : 3 (1) With no branch Cycle number :5 Timing : ø SYNC R/W RD WR ADDR PC PC+1 ADL,00 PC+2 ADL DATA Op-code DATA Invalid ADDRH РСн РСн 00 РСн ADDRL Op-code In-valid In-valid PCL+1 ADL DATA PCL ADL PCL+2 PCL+2 /DATA

## **BIT RELATIVE**

Instructions	: ∆BBC∆i,\$zz,\$hhll ∆BBS∆i,\$zz,\$hhll
Byte length	: 3
(2) With bran Cycle number	ch : 7
Timing	:
ф	
SYNC	
R/W	
RD	
WR	
ADDR	$ \begin{array}{ c c c c c } \hline PC & PC+1 & ADL,00 & PC+2 & \begin{pmatrix} (PC+3)L \\ (PC+2)H & (PC+3) \pm RR \end{pmatrix} & \begin{pmatrix} (PC+3) \pm RR \\ \pm RR \end{pmatrix} \\ \hline \end{array} $
DATA	Op-code ADL DATA Invalid ±RR Invalid Invalid
ADDRH	PCH PCH 00 PCH (PC+2)H (PC+3)H ((PC+3) ± RR)H
ADDRL /DATA	PCL Code PCL+1 ADL ADL DATA PCL+2 In- valid PCL+2 ±RR *1 (*2) (*2)
RR : Offset	address

\*1 : (PC+3)L \*2 : ((PC+3)±RR)L

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## **ZERO PAGE BIT**

: ∆CLB∆i,\$zz
∆SEB∆i,\$zz
: 2
: <b>5</b>

:

Timing



[T=0]		ZERO PAGE
Instructions :	AADCA\$zzAANDA\$zzABITA\$zzACMPA\$zzACPYA\$zzACPYA\$zzACPYA\$zzALDAA\$zzALDXA\$zzALDYA\$zzACPYA\$zzALDXA\$zzALDYA\$zzACDYA\$zzALDYA\$zzACDYA\$zzACDYA\$zzACDYA\$zzACDYA\$zzACDYA\$zzACDYA\$zzACDYA\$zzACDYA\$zzACDYA\$zzACSBCA\$zzACSTA\$zz	(T=0) (T=0) (T=0) (T=0) (T=0) (T=0)
Byte length :: Cycle number ::	2 3	
Timing :		
¢ Sync		
R/W		
RD		
ADDR	PC	PC+1 ADL,00
DATA	Op-coc	de ADL DATA
ADDRH	РСН	РСН 00
ADDRL /DATA	PCL Op-	CL+1 ADL ADL DATA

Instructions :  $\triangle ASL \ \triangle Szz \ \triangle COM \ \triangle Szz \ \triangle DEC \ \triangle Szz \ \triangle INC \ \triangle Szz \ \triangle INC \ \triangle Szz \ \triangle LSR \ \triangle Szz \ \triangle ROL \ 2 \ Szz \ Cycle number : 5$ 

:

Timing

ø SYNC R/W RD WR ADDR PC PC+1 ADL,00 NEW DATA Op-code ADL DATA Invalid DATA ADDRH РСн РСн 00 ADDRL Op-code NEW DA TA PCL ADL ADL DATA ADL PCL+1 ADL /DATA

## ZERO PAGE

Instruction Byte lengt Cycle num	i ∴ ∆ <b>RRF∆\$zz</b> h : <b>2</b> nber : <b>8</b>		
Timing	:		
ф			
SYNC			
R/W			
RD			
WR			
addr 🔇	PC PC+1	ADL,00	
DATA	Op-code ADL DATA	Invalid	NEW DATA
addrh 🔇	РСН РСН	00	
ADDRL	PCL Op- wde PCL+1 ADL ADL DATA ADL -		ADL NEW DA TA

## **ZERO PAGE**





# Zero Page X

Instructio Byte leng Cycle nu	on gth mber	: ∆MUL∆\$zz,X : 2 : 15	(Note)
Timing		:	
ф			
SYNC			
R/W			
RD			
WR			
ADDR	(PC)	PC+1	ADL+X,00 X S,SPS X
DATA	Op- code		Invalid (NEW DATA Valid)

SPS: A selected page by stack page selection bit of the CPU mode register.

Note: This instruction cannot be used for some products.

# Zero Page X

Instructio Byte len Cycle nu	on gth umber	: ∆DIV∆\$zz,X : 2 : 16	(Note)	
Timing		:		
ф				
SYNC				
R/W				
RD				
WR				
ADDR	PC F	PC+1 ADL +X,00	ADL+X+1,00	S,SPS
DATA	Op- code			NEW In- Valid

SPS: A selected page by stack page selection bit of the CPU mode register.

Note: This instruction cannot be used for some products.

Zero Page X		
Instructions : A A A A	ASL Δ\$zz,X DEC Δ\$zz,X INC Δ\$zz,X LSR Δ\$zz,X ROL Δ\$zz,X	
Byte length : 2 Cycle number : 6	κυκΔφΖΖ,λ	
Timing :		
φ <b>SYNC</b>		
R/W		
RD		
WR		
ADDR	PC PC+1 (PC+1)L ADL+X,00	
DATA	Op-code ADL Invalid DATA Invalid NEW DATA	
ADDRH	PCH PCH 00	
ADDRL /DATA	PCL Op- wde PCL+1 (ADL (PC+1)L) (ADL+X (DATA (ADL+X) (ADL+X (DATA (ADL+X)))))	


## ZERO PAGE X, ZERO PAGE Y



[T=0]

		( <b>—</b> )	
Instructions	:Δ <b>ADC</b> Δ\$hhll	(T=0)	
	∆AND ∆\$hhll	(T=0)	
	∆ <b>BIT</b> ∆\$hhll		
	∆CMP ∆\$hhll	(T=0)	
	∆CPX ∆\$hhll	. ,	
	∆CPY ∆\$hhll		
	∆EOR ∆\$hhll	(T=0)	
	∆LDA ∆\$hhll	(T=0)	
	∆LDX ∆\$hhll	( )	
	∆LDY ∆\$hhll		
	∆ORA ∆\$hhll	(T=0)	
	∧SBC ∧\$hhll	(T=0)	
Ryte length	• 3	(,	
Cycle nymher			
Cycle number	. 4		

:

Timing



## ABSOLUTE



### ABSOLUTE



#### ABSOLUTE



Note: Some products are "01" or content of SPS flag.

Instructions	: Δ <b>STA</b> Δ Δ <b>STX</b> Δ Δ <b>STX</b> Δ	\$hhll \$hhll \$bbll
Byte length Cycle number	: 3 : 5	φ
Timing	:	
	φ	
	SYNC	
	R/W	
	RD	
	WR	
	ADDR	PC PC+1 PC+2 ADL ADL ADH
	DATA	Op-code ADL ADH Invalid DATA
	ADDRH	PCH PCH PCH ADH
	ADDRL /DATA	PCL Op- code PCL+1 ADL PCL+2 ADH ADL ADL DATA

[T=0]

## ABSOLUTE X, ABSOLUTE Y

Instructions	: ΔΑΕ ΔΑΝ ΔCΝ ΔEC ΔLD ΔLD ΔLD ΔCF ΔSF	PC $\Delta$ \$hhll,X or Y (T=0) ID $\Delta$ \$hhll,X or Y (T=0) IP $\Delta$ \$hhll,X or Y (T=0) IR $\Delta$ \$hhll,X or Y (T=0) A $\Delta$ \$hhll,X or Y (T=0) X $\Delta$ \$hhll,X Y $\Delta$ \$hhll,X C $\Delta$ \$hhll,X or Y (T=0) C $\Delta$ \$hhll,X or Y (T=0)	
Byte length Cycle number	: 3 : 5		
Timing	:		
	ф		
	SYNC		
	R/W		
	RD		
	WR		
	ADDR	PC PC+1 PC+2 AD L+X(or Y) AD L+X(or Y) AD H+C AD H+C	$\rangle$
	DATA	Op-code ADL ADH Invalid DATA	
A	DDRH	PCH PCH PCH ADH ADH +C	
P I	ADDRL /DATA	(PCL) (Op- code) (PCL+1) (ADL) (PCL+2) (ADH) (Or Y) (ADL+X) (Or Y) (DATA) (ADL+X) (Or Y) (DATA) (ADL+X) (A	
	$\sim \sim \sim \sim$		

C : Carry of ADL+X or Y

#### **ABSOLUTE X**

Instructions	: ΔASL Δ\$hhll,X ΔDEC Δ\$hhll,X ΔINC Δ\$hhll,X ΔLSR Δ\$hhll,X ΔROL Δ\$hhll,X ΔROR Δ\$hhll,X
Byte length	: 3 or : 7
Timing	
φ	
SYNC	
R/W	
RD	
WR	
ADDR	PC PC+1 PC+2 ADL+X ADL+X ADL+X ADH+C
DATA	Op-code ADL ADH Invalid DATA Invalid NEW DATA
ADDRH	PCH PCH PCH ADH ADH+C
ADDRL /DATA	(PCL) Op- WCL+1) ADL (PCL+2) ADH (ADL+X) (ADL+X) (DATA) (ADL+X) (ADL+X) (NEW)

 $C: C \text{ any of } \mathsf{ADL}\text{+}\mathsf{X}$ 

## **ABSOLUTE X, ABSOLUTE Y**



C : Carry of ADL+X or Y

#### **INDIRECT**



#### **ZERO PAGE INDIRECT**



BA : Basic address

## ZERO PAGE INDIRECT



BA : Basic address

Note: Some kind types are "01" or content of SPS flag.

ſŢ	=01	
լս		

**INDIRECT X** 

Instructions	: $\triangle ADC \ \triangle(\$zz,X)$ (T=0) $\triangle AND \ \triangle(\$zz,X)$ (T=0) $\triangle CMP \ \triangle(\$zz,X)$ (T=0) $\triangle EOR \ \triangle(\$zz,X)$ (T=0) $\triangle LDA \ \triangle(\$zz,X)$ (T=0) $\triangle ORA \ \triangle(\$zz,X)$ (T=0) $\triangle SBC \ \triangle(\$zz,X)$ (T=0)
Byte length Cycle number	: <b>2</b> : <b>6</b>
Timing	:
φ	
SYNC	
R/W	
RD	
WR	
ADDR	PC PC+1 (PC+1) L,00 BAL+X,00 BAL+X+1 ADL ADH ADH
DATA	Op-code BAL Invalid ADL ADH DATA
ADDRH	PCH PCH 00 ADH
ADDRL /DATA	(PCL Code PCL+1 BAL PCL+1 BAL PCL+1 BAL PCL+1) BAL+X ADL BAL ADL ADL ADL DATA

BA : Basic address

#### **INDIRECT X**



BA : Basic address

	T	=01	
Ļ,	U		

**INDIRECT Y** 

Instructions	: $\triangle ADC \triangle (\$zz), Y$ (T=0) $\triangle AND \triangle (\$zz), Y$ (T=0) $\triangle CMP \triangle (\$zz), Y$ (T=0) $\triangle EOR \triangle (\$zz), Y$ (T=0) $\triangle LDA \triangle (\$zz), Y$ (T=0) $\triangle ORA \triangle (\$zz), Y$ (T=0) $\triangle SBC \triangle (\$zz), Y$ (T=0)
Byte length Cycle numb	: 2 er : 6
Timing	:
φ	
SYNC	
R/W	
RD	
WR	
ADDR	PC PC+1 BAL,00 BAL+1 ADL+Y ADL+Y ADL+Y ADH+C
DATA	Op-code BAL ADL ADH Invalid DATA
ADDRH	PCH PCH 00 ADH ADH+C

 $\mathbf{X}^{-}$ 

BA : Basic address

PCL

Opœde

PCL+1

BAL

BAL

ADL BAL+1

ADL+Y

ADH

ADL+Y

DATA

ADDRL

/DATA

C : Carry of ADL+Y

## **INDIRECT Y**

Instructio Byte leng Cycle nu	n jth mber	: ΔSTAΔ(\$zz),Y : 2 : 7
Timing		:
ф		
SYNC		
R/W		
RD		
WR		
ADDR	PC	PC+1 BAL,00 BAL+1 ADL+Y ADL+Y ADL+Y ADL+Y ADH+C
DATA		Dp-code BAL ADL ADH Invalid Invalid DATA
ADDRH	РСн	PCH 00 ADH ADH+C
ADDRL /DATA		Dp- de PCL+1 ADL BAL ADL ADL ADL ADL ADL ADL ADL ADL ADL A

BA : Basic address

C : Carry of ADL+Y

Instructions	: ΔBCC ΔBCS ΔBEQ ΔBMI ΔBNE ΔBNE ΔBPL ΔBVC ΔBVS	Δ\$hhll Δ\$hhll Δ\$hhll Δ\$hhll Δ\$hhll Δ\$hhll Δ\$hhll Δ\$hhll
Byte length	: 2	
(1)With no branch Cycle number	: 2	
Timing	:	
	φ	
	SYNC	
	R/W	
	RD	
	WR	
	ADDR	PC PC+1
	DATA	Op-code Invalid
Д	DDRH	РСН РСН
	ADDRL /DATA	PCL Op- wde PCL+1 In- valid

Instructions	: ΔBCC ΔBCS ΔBEQ ΔBMI ΔBNE ΔBNE ΔBVC ΔBVS	A\$hhll Δ\$hhll Δ\$hhll Δ\$hhll Δ\$hhll Δ\$hhll Δ\$hhll Δ\$hhll
Byte length	: <b>2</b>	
(2)With branch Cycle number	: 4	
Timing	:	
	φ	
	SYNC	
	R/W	
	RD	
	WR	
	ADDR	$\begin{array}{ c c c c c } \hline PC & PC+1 & (PC+2)L \\ PC+1)H & (PC+2) \pm RR)L \\ (PC+2)H & (PC+2) \pm RR \\ PC+2 & H \\ \hline \hline PC+2 & H \\ \hline PC+2 & H \\ \hline \hline PC+2 & H \\ \hline$
	DATA	Op-code ±RR Invalid Invalid
Ą	DDRH	PCH PCH (PC+1)H (PC+2)H ((PC+2)±RR)H (PC+2)±RR)H
	ADDRL /DATA	$ \left( \begin{array}{c} PCH \\ Code \\ PCL+1 \\ \end{array} \right) \stackrel{\pm}{=} RR \\ RR \\ RR \\ PC+2 \\ RR $
-		

RR : Offset value

#### RELATIVE



RR : Offset value

#### **SPECIAL PAGE**



BA : Basic address

Note : Some products are "01" or content of SPS flag.

**IMMEDIATE** 



#### **IMMEDIATE**



#### **IMMEDIATE**



[T=1]	ZERO PAGE
Instructions	: ΔADCΔ\$zz (T=1) ΔANDΔ\$zz (T=1) ΔEORΔ\$zz (T=1) ΔORAΔ\$zz (T=1) ΔSPCΔ\$zz (T=1)
Byte length Cycle number	: 2 : 6
Timing	:
φ	
SYNC	
R/W	
RD	
WR	
ADDR	PC PC+1 ADL,00 X,00 X
DATA	Op-code ADL DATA DATA Invalid NEW DATA
ADDRH	PCH PCH 00
ADDRL /DATA	$\left\langle PCL \right\rangle \left\langle \begin{array}{c} Op \\ ode \end{array} \right\rangle \left\langle PCL+1 \right\rangle \left\langle ADL \right\rangle \left\langle ADL \right\rangle \left\langle \begin{array}{c} DATA \\ 1 \end{array} \right\rangle \left\langle X \right\rangle \left\langle \begin{array}{c} DATA \\ 2 \end{array} \right\rangle \left\langle X \right\rangle \left\langle X \right\rangle \left\langle \begin{array}{c} NEW \\ DATA \end{array} \right\rangle \left\langle X \right\rangle \right\rangle$

$$[T=1]$$

**ZERO PAGE** 





**ZERO PAGE X** 

: ΔADCΔ\$zz,X ΔANDΔ\$zz,X ΔEORΔ\$zz,X ΔORAΔ\$zz,X	(T=1) (T=1) (T=1) (T=1)
∴SBC∆\$22,X : 2 : 7	(1=1)
	: ΔADCΔ\$zz,X ΔANDΔ\$zz,X ΔEORΔ\$zz,X ΔORAΔ\$zz,X ΔSBCΔ\$zz,X : 2 : 7

:

Timing





**ZERO PAGE X** 





[T=1	] ABSOLUTE
Instruction	ns : ΔADCΔ\$hhll (T=1) ΔANDΔ\$hhll (T=1) ΔEORΔ\$hhll (T=1) ΔORAΔ\$hhll (T=1) ΔSBCΔ\$hhll (T=1)
Byte leng Cycle nur	th : 3 nber : 7
Timing	:
ф	
SYNC	
R/W	
RD	
WR	
ADDR	PC PC+1 PC+2 ADL X,00
DATA	Op-code ADL ADH DATA DATA 2 Invalid DATA
ADDRH	PCH PCH PCH ADH 00
ADDRL /DATA	(PCL Code PCL+1 ADL PCL+2 ADH ADL DATA X DATA X ADATA

#### ABSOLUTE

Instruction Byte length Cycle number	: ΔCMP∆\$hhll (T=1) : 3 : 5
Timing	:
φ	
SYNC	
R/W	
RD	
WR	
ADDR	PC PC+1 PC+2 ADL X,00
DATA	Op-code ADL ADH ADH DATA DATA 2
ADDRH	PCH PCH PCH ADH 00
ADDRL /DATA	PCL Op- code PCL+1 ADL PCL+2 ADH ADL DATA 1 X DATA 2

ABSOLUTE



## ABSOLUTE X, ABSOLUTE Y

Instructio	ons	: ΔADCΔ\$hhi ΔANDΔ\$hhi ΔEORΔ\$hhi ΔORAΔ\$hh ΔSBCΔ\$hhi	II,X or Y II,X or Y II,X or Y II,X or Y II,X or Y	(T=1) (T=1) (T=1) (T=1) (T=1)				
Byte len	igth	: 3						
Cycle nu	umber	: 8						
Timing		:						
φ								
SYNC								
R/W								
RD								
WR								
ADDR	PC	PC+1	PC+2	DL+X(or Y) ADH ADH	+X(or Y) H+C	X,00		
DATA		-code ADL	ADH	Invalid		DATA 2	Invalid	NEW DATA
ADDRH	РСн	РСН	РСН	ADH AD	н+С	0	0	
ADDRL /DATA				ADL+X (or Y)		DATA 2 X	{ ×	NEW DA TA
C:Carry	of ADL+X or	Y						

# [T=1]ABSOLUTE X, ABSOLUTE Y

Instruction Byte length Cycle numb	: △CMP∆\$hhll,X or Y (T=1) : 3 er : 6
Timing	:
φ	
SYNC	
R/W	
RD	
WR	
ADDR	PC PC+1 PC+2 ADL+X(or Y) ADL+X(or Y) X,00 X,00
DATA	Op-code ADL ADH Invalid DATA DATA 2
ADDRH	PCH PCH PCH ADH ADH+C 00
ADDRL /DATA	$\left( \begin{array}{c} PCL \\ \infty de \end{array} \right) \left( \begin{array}{c} Op-\\ PCL+1 \\ \end{array} \right) \left( \begin{array}{c} ADL \\ PCL+2 \\ \end{array} \right) \left( \begin{array}{c} ADL+X \\ (or Y) \\ \end{array} \right) \left( \begin{array}{c} ADL+X \\ (or Y) \\ \end{array} \right) \left( \begin{array}{c} DATA \\ 1 \\ \end{array} \right) \left( \begin{array}{c} ADTA \\ 2 \\ \end{array} \right) \left( \begin{array}{c} DATA \\ 2 \\ \end{array} \right) \left( \begin{array}{c} DAT$

C : Carry of ADL+X or Y

## **ABSOLUTE X, ABSOLUTE Y**

Instruction	: ∆LDA∆\$hhll,X or Y	(T=1)
Byte length	: 3	
Cycle number	:7	

Timing

[T=1]



C : Carry of ADL+X or Y

INDIRECT X
: ΔADCΔ(\$zz,X) (T=1) ΔANDΔ(\$zz,X) (T=1) ΔEORΔ(\$zz,X) (T=1) ΔORAΔ(\$zz,X) (T=1) ΔSRCΔ(\$zz,X) (T=1)
: 2 er : 9
:
$ \left( \begin{array}{c} PC \\ PC+1 \\ \begin{array}{c} PC+1 \\ \end{array} \end{array} \right)} \right) $
Op- code BAL XInvalid ADL X ADH X DATA 2 Invalid NEW DATA
PCH PCH 00 ADH 00 (ADH)
(PCL) Code PCL BAL (PC +1)L (BAL AD L) BAL+ AD H AD L DATA X

BA : Basic address


BA : Basic address

# [T=1]

**INDIRECT X** 



BA : Basic address



**INDIRECT Y** 



C : Carry of ADL+Y

## [T=1]

**INDIRECT Y** 



BA : Basic address

C : Carry of ADL+Y



#### **INDIRECT Y**



BA : Basic address

C : Carry of ADL+Y

#### **APPENDIX 2. 740 Family Machine Language Instruction Table**

Parameter		0/400		NOTION	FLAG	INSTRUCTION CO	BYTE	CYCLE		
Classi	ification	SYMBOL	FU	NCTION	NVTBDIZC	D7D6D5D4 D3D2D1D0	NUMBER	NUMBER	NOTE	
		LDA #\$nn	(A)←nn		$\bigcirc$ x x x x x $\bigcirc$ x	1010_1001	A9	2	2	2
		LDA \$zz	(A)←(M) where	M=(zz)	$\bigcirc$ x x x x x $\bigcirc$ x	<b2> 1010_0101</b2>	A5	2	3	2
		LDA \$zz, X	(A)←(M) where	M=(zz+(X))	$\bigcirc$ x x x x x $\bigcirc$ x	<b2> 1011_0101</b2>	B5	2	4	2
		LDA \$ hhll	(A)←(M) where	M=(hhll)	$\bigcirc$ x x x x x $\bigcirc$ x	<b2> 1010 1101</b2>	AD	3	4	2
						<b2> <b3></b3></b2>				
		LDA \$ hhll, X	(A)←(M) where	M=(hhll+(X))	$\bigcirc$ X X X X $\bigcirc$ X	1011 1101 <b2></b2>	BD	3	5	2
		LDA \$ hhll, Y	(A)←(M) where	M=(hhll+(Y))	0xxxxx0x	<b3> 1011 1001</b3>	B9	3	5	2
						<b2> <b3></b3></b2>				
		LDA (\$ zz, X)	(A)←(M) where	M=((zz+(X)+1)(zz+(X)))	$\bigcirc$ x x x x x $\bigcirc$ x	10100001 <b2></b2>	A1	2	6	2
		LDA (\$ zz), Y	(A)←(M) where	M=((zz+1)(zz)+(Y))	()XXXXX()X	1011 0001 <b2></b2>	B1	2	6	2
	g	LDX #\$nn	(X)←nn		$\bigcirc$ x x x x x $\bigcirc$ x	1010 0010	A2	2	2	
	Lo	LDX \$zz	(X)←(M) where	M=(zz)	$\bigcirc$ x x x x x $\bigcirc$ x	10100110	A6	2	3	
		LDX \$zz, Y	(X)←(M) where	M=(zz+(Y))	$\bigcirc$ x x x x x $\bigcirc$ x	10110110	B6	2	4	
		LDX \$ hhll	(X)←(M) where	M=(hhll)	$\bigcirc$ x x x x x $\bigcirc$ x	<b2> 101011110</b2>	AE	3	4	
		IDX \$ hhll Y	(X)←(M) where	M=(hhll+(Y))		<b2> <b3></b3></b2>	BE	3	5	
		2077 <b>Q</b> 1111, 1				<pre></pre>				
		LDY #\$nn	(Y)←nn		$\bigcirc$ x x x x x $\bigcirc$ x	1010_0000	A0	2	2	
ata Transfer		LDY \$ zz	(Y)←(M) where	M=(zz)	$\bigcirc$ x x x x x $\bigcirc$ x	<b2> 1010_0100</b2>	A4	2	3	
		LDY \$zz, X	(Y)←(M) where	M=(zz+(X))	$\bigcirc$ x x x x x $\bigcirc$ x	<b2> 1011 0100</b2>	B4	2	4	
		LDY \$ hhll	(Y)←(M) where	M=(hhll)	$\bigcirc$ x x x x x $\bigcirc$ x	<b2> 1010_1100</b2>	AC	3	4	
						<b2> <b3></b3></b2>				
		LDY \$ hhll, X	(Y)←(M) where	M=(hhll+(X))	$\bigcirc$ x x x x x $\bigcirc$ x	10111100 <b2></b2>	BC	3	5	
		LDM #\$nn,\$zz	(M)←nn where	M=(zz)		<b3></b3>	3C	3	4	
Ő						<b2> <b3></b3></b2>				
		STA \$zz	(M)←(A) where	M=(zz)	*****	1000 0101 <b2></b2>	85	2	4	
		STA \$zz, X	(M)←(A) where	M=(zz+(X))	******	1001 0101 -B2>	95	2	5	
		STA \$ hhll	(M)←(A) where	M=(hhll)	******	1000 1101	8D	3	5	
		STA ¢ bbll Y		$M_{-}(bbll_{+}(Y))$		<b3></b3>	00	2	6	
		STA \$1111, A		₩=(IIIII+(X))		<b2></b2>	30	5		
		STA \$ hhll, Y	(M)←(A) where	M=(hhll+(Y))	******	1001 1001 -B25	99	3	6	
		STA (\$ 77 X)	(M)←(A) where	M=((77+(X)+1)(77+(X)))		<b3></b3>	81	2	7	
		STA (\$ 77) Y	(M) (A) where	M = ((zz+1)(zz)+(Y))	~~~~~~~	<b2> 1001001</b2>	91	2	7	
	to Te	STX \$ 77	(M)((X) where	M=((22+1)(22)+(1))	~~~~~~	<b2></b2>		-		
	Ó	STX \$ 77 Y	(M)←(X) where	M=(ZZ+(Y))	******	1000 0110 <b2></b2>	86	2	4	
		STX \$ bbll	(M)←(X) where	M=(bbll)	******	1001 0110 <b2></b2>	96	2	5	
				m=(nm)	******	1000 1110 <b2></b2>	8E	3	5	
	-	STY \$ 77	(M) (Y) where	M=(77)	*****	<b3></b3>	84	2	4	
		STY \$ 77 X	(M)←(Y) where	M = (zz + (X))	*****	<b2></b2>	94	2	5	
		STY \$ bbll	(M)←(Y) where	M=(bbll)	*****	<b2></b2>	8C	3	6	
		orr orm		-(IIII)		<b2> <b3></b3></b2>				
	er	TAX TXA	$(X) \leftarrow (A)$ $(A) \leftarrow (X)$		$\bigcirc x \times x \times x \bigcirc x \\ \bigcirc x \times x \times x \bigcirc x \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\$	1010 1010 1010	AA 8A	1	2	
	nsf	TAY	(Y)←(A)			1010 1000	A8	1	2	
	Tra	TSX	(A)←(T) (X)←(S)		$\bigcirc X X X X \bigcirc X \\ \bigcirc X X X X X \bigcirc X \\ \bigcirc$	1011 1010	98 BA	1	2	
		TXS PHA	$(S) \leftarrow (X)$	s)—1	XXXXXXXXXX	1001 1010	9A	1	2	<u> </u>
	ack	PHP	(M(S))←(PS), (S)←	,, S)—1	x x x x x x x x x	0000 1000	48 08	1	3	
	Ope St	PLA PLP	(S)←(S)+1, (A)←(M (S)←(S)+1, (PS)←(	(S)) M(S))	OXXXXXOX Previous status in stack	0110 1000 0010 1000	68 28	1	4	

RENESAS

Parameter Classification		0)// 40 01			FLAG	INSTRUCTION C	ODE	BYTE	CYCLE	NOTE
		SYMBOL	FUNG	TION	NVTBDIZC	D7D6D5D4 D3D2D1D0	HEX	NUMBER	NUMBER	NOTE
		ADC #\$nn	(A)←(A)+nn+(C)		00 <b>x</b> x x x 00	01101001	69	2	2	1
		ADC \$zz	(A)←(A)+(M)+(C) where	M=(zz)	00××××00	01100101	65	2	3	1
		ADC \$zz, X	(A)←(A)+(M)+(C) where	M=(zz+(X))	00××××00	<в2> 01110101	75	2	4	1
		ADC \$ hhll	(A)←(A)+(M)+(C) where	M=(hhll)	00××××00	01101101	6D	3	4	1
		ADC \$ hhll, X	(A)←(A)+(M)+(C) where	M=(hhll+(X))	00××××00	<b2> <b3> 0 1 1 1 1 0 1 <b2></b2></b3></b2>	7D	3	5	1
		ADC \$ hhll, Y	(A)←(A)+(M)+(C) where	M=(hhll+(Y))	00××××00	<b3> 0 1 1 1 1 0 0 1 <b2></b2></b3>	79	3	5	1
		ADC (\$ zz, X)	(A)←(A)+(M)+(C) where	M=((zz+(X)+1)(zz+(X)))	00××××00	<вз> 0110_0001	61	2	6	1
		ADC (\$ zz), Y	(A)←(A)+(M)+(C) where	M=((zz+1)(zz)+(Y))	00××××00	<pre> <b2> 0 1 1 1 0 0 0 1 <b2></b2></b2></pre>	71	2	6	1
		SBC #\$nn	(A)←(A)–nn–(C)		00××××00	1 1 1 0 1 0 0 1 <b2></b2>	E9	2	2	1
		SBC \$zz	$(A) \leftarrow (A) - (M) - (\overline{C})$ where $M = (zz)$		00××××00	1 1 1 0 0 1 0 1 <b2></b2>	E5	2	3	1
		SBC \$zz, X	(A)←(A)–(M)–(C) where	M=(zz+(X))	00××××00	1 1 1 1 0 1 0 1 <b2></b2>	F5	2	4	1
		SBC \$ hhll	$(A) \leftarrow (A) - (M) - (\overline{C})$ where	M=(hhll)	00××××00	1 1 1 0 1 1 0 1	ED	3	4	1
eration	truct	SBC \$ hhll, X	(A)←(A)–(M)–(C) where	M=(hhll+(X))	00****00	<b3> 1 1 1 1 1 1 0 1 <b2></b2></b3>	FD	3	5	1
	Sabs	SBC \$ hhll, Y	(A)←(A)−(M)−(C) where	M=(hhll+(Y))	00****00	<b3> 1 1 1 1 1 0 0 1 <b2></b2></b3>	F9	3	5	1
	Add and	SBC (\$ zz, X)	(A)←(A)−(M)−(C) where	M=((zz+(X)+1)(zz+(X)))	00××××00		E1	2	6	1
		SBC (\$ zz), Y	(A)←(A)–(M)–(C) where	M=((zz+1)(zz)+(Y))	00××××00	<b2> 1 1 1 1 0 0 0 1 <b2></b2></b2>	F1	2	6	1
ope		INC A	(A)←(A)+1		0 x x x x x 0 x	0011 1010	3A	1	2	-
		INC \$zz	(M)←(M)+1 where	1 where M=(zz)		1110 0110	E6	2	5	
		INC \$zz, X	(M)←(M)+1 where	M=(zz+(X))	$\bigcirc$ x x x x x $\bigcirc$ x	<b2> 1 1 1 1 0 1 1 0</b2>	F6	2	6	
		INC \$ hhII (M)←(M)+1 where		M=(hhll)	0 x x x x x 0 x	<b2> 1 1 1 0 1 1 1 0 <b2></b2></b2>	EE	3	6	
		INC \$ hhll, X	(M)←(M)+1 where M=(hhll+(X))		$\bigcirc$ x x x x x $\bigcirc$ x	<b3> 1 1 1 1 1 1 1 0 <b2> <b3></b3></b2></b3>	FE	3	7	
		DEC A	(A)←(A)−1		$\bigcirc$ x x x x x $\bigcirc$ x	0001 1010	1A	1	2	
		DEC \$zz	(M)←(M)−1 where	M=(zz)	$\bigcirc$ x x x x x $\bigcirc$ x	1100 0110 <b2></b2>	C6	2	5	
		DEC \$zz, X	(M)←(M)−1 where	M=(zz+(X))	$\bigcirc$ x x x x x $\bigcirc$ x	1 1 0 1 0 1 1 0	D6	2	6	
		DEC \$ hhll	(M)←(M)−1 where	M=(hhll)	OxxxxxOx	1 1 0 0 1 1 1 0 <b2></b2>	CE	3	6	
		DEC \$ hhll, X	(M)←(M)−1 where	M=(hhll+(X))	○×××××⊙×	<pre> <b3>     1 1 0 1 1 1 1 0         <b2>         <b3>     </b3></b2></b3></pre>	DE	3	7	
		INX	(X)←(X)+1		$\bigcirc$ x x x x x $\bigcirc$ x	1110 1000	E8	1	2	
		DEX	(X)←(X)−1		$\bigcirc$ x x x x x $\bigcirc$ x	1100 1010	CA	1	2	
		INY	(Y)←(Y)+1		$\bigcirc$ x x x x $\bigcirc$ x	1100 1000	C8	1	2	
		DEY	(Y)←(Y)−1		$\bigcirc$ x x x x x $\bigcirc$ x	1000 1000	88	1	2	
	tiply /ide	MUL \$zz, X	$\begin{array}{c} M(S),(A)\leftarrow(A)XM(zz+(X))\\ (S)\leftarrow(S)-1 \end{array}$		*****	0110 0010	62	2	15	
Multi		DIV \$zz, X	$(A) \leftarrow (M(zz+(X)+1), M(zz+(X) + M(S)) \leftarrow One's complement of (S) \leftarrow (S) - 1$	))÷(A) Fremainder	*****	1110 0010	E2	2	16	

Parameter		SVMPOL					FLAG	INSTRUCTION C	ODE	BYTE	CYCLE	
Classification		STMBOL	FUNCTION		NVTBDIZC	D7D6D5D4 D3D2D1D0	HEX	NUMBER	NUMBER	NOTE		
	AND #\$nn		(A)←(A)^	nn			OxxxxxOx	0010 1001	29	2	2	1
		AND \$zz	(A)←(A)∧	(M)	where	M=(zz)	0 x x x x x 0 x	<b2> 0010 0101</b2>	25	2	3	1
		AND \$zz, X	(A)←(A)∧	(M)	where	M=(zz+(X))	0 x x x x x 0 x	<b2> 0011 0101</b2>	35	2	4	1
		AND \$ hhll	(A)←(A)^	(M)	where	M=(hhll)	0 x x x x x 0 x	<b2> 0010 1101</b2>	2D	3	4	1
								<b2> <b3></b3></b2>				
		AND \$ hhll, X	(A)→(A)	. (M)	where	M=(hhII+(X))	0 x x x x x 0 x	0011 1101 <b2></b2>	3D	3	5	1
		AND \$ hhll, Y	(A)←(A)∧	(M)	where	M=(hhll+(Y))	0 × × × × × 0 ×	<b3> 0 0 1 1 1 0 0 1</b3>	39	3	5	1
				(M)	whore	$M_{-}(77+(Y)+1)(77+(Y)))$		<b2> <b3></b3></b2>				
		AND (\$ 22, X)	$(A) \leftarrow (A)$	(A)←(A)∧ (M) where		$M_{-((22+(X)+1)(22+(X)))}$		<pre></pre>	21		0	
		AND (\$ 22), I		(101)	where	WI=((22+1)(22)+(1))	0	<pre></pre>	31	2	0	<u>'</u>
ion		ORA #\$nn	(A)→(A)	(A)←(A)∨(M)			$\bigcirc$ X X X X X $\bigcirc$ X	00001001 <b2></b2>	09	2	2	1
		ORA \$zz	(A)→(A)	(A)←(A)√(M) wh		M=(zz)	$\bigcirc$ x x x x x $\bigcirc$ x	00000101 <b2></b2>	05	2	3	1
		ORA \$zz, X	(A)→(A)	(A)←(A)∨(M) W		M=(zz+(X))	$\bigcirc$ x x x x x $\bigcirc$ x	00010101 <b2></b2>	15	2	4	1
	_	ORA \$ hhll	(A)→(A)	(M)	where	M=(hhll)	$\bigcirc$ x x x x x $\bigcirc$ x	00001101 <b2></b2>	0D	3	4	1
	atior	ORA \$ hhll, X	(A)←(A)∨	·(M)	where	M=(hhll+(X))	OxxxxxOx	<b3> 0 0 0 1 1 1 0 1 <b2></b2></b3>	1D	3	5	1
	pera	ORA \$ hhll, Y	(A)←(A)∨	(A)→(A)→(A)		M=(hhll+(Y))	$\bigcirc$ x x x x x $\bigcirc$ x	<b3> 0 0 0 1 1 0 0 1</b3>	19	3	5	1
	0 0		$(\Delta) \leftarrow (\Delta)_{\mathcal{V}}$	(A)←(A)∨(M) wh		M-((77+(X)+1)(77+(X)))		<b2> <b3></b3></b2>	01	2	6	1
	ogi	ORA $(522, \Lambda)$	(A)←(A)∨ (A)←(A)∨	$(A) \leftarrow (A) \lor (M)$ when		M = ((zz+(X)+1)(zz+(X)))		<pre></pre>	11	2	6	
				(m) /nn			0	<b2></b2>	10	2	2	1
		EOR #\$nn	(A)←(A) ∨	nn ((M)	where	M ()		<pre></pre>	49		2	
		EUR \$ 22	(A)←(A)∨	(IVI) ((MA)	where	M = (22)		<pre></pre>	45		1	
		EOR \$ ZZ, X	(A)←(A) ∨	(1VI)	where	M=(22+(X))		<pre></pre>	55	2	4	
		EOR \$ nnii	(A)←(A) ⊽	(111)	wnere	M=(nnii)		<pre><b2> <b3></b3></b2></pre>	4D	3	4	'
		EOR \$ hhll, X	(A)→(A)∀	′(M)	where	M=(hhll+(X))	$\bigcirc$ x x x x x $\bigcirc$ x	0 1 0 1 1 1 0 1 <b2></b2>	5D	3	5	1
pera		EOR \$ hhll, Y	(A)←(A)∀	′(M)	where	M=(hhll+(Y))	$\bigcirc x \times x \times x \bigcirc x$	<b3> 0 1 0 1 1 0 0 1 <b2></b2></b3>	59	3	5	1
ō		EOR (\$ zz, X)	(A)←(A)∀	(A)→(A)		M=((zz+(X)+1)(zz+(X)))	$\circ$ x x x x x $\circ$ x	<b3> 0 1 0 0 0 0 0 1</b3>	41	2	6	1
		EOR (\$ zz), Y	(A)←(A)∀	(A)←(A)∀(M)		M=((zz+1)(zz)+(Y))	$\bigcirc$ x x x x x $\bigcirc$ x	<b2> 0 1 0 1 0 0 0 1 <b2></b2></b2>	51	2	6	1
		COM \$ zz	(M)→(M)	$(\overline{M}){\rightarrow}(M)$		M=(zz)	$\bigcirc$ x x x x x $\bigcirc$ x	01000100 <b2></b2>	44	2	5	
		BIT \$ zz	(A) ^ (M)		where	M=(zz)	M7M6X X X X 🔿 X	00100100	24	2	3	
		BIT \$ hhll	(A) ^ (M)		where	M=(hhll)	M7M6X X X X 🔿 X	00101100	2C	3	4	
								<b2> <b3></b3></b2>				
		TST \$zz	(M)=0?	_	where	M=(zz)	0 x x x x x 0 x	01100100 <b2></b2>	64	2	3	
		CMP #\$nn	(A)–nn				0×××××00	1 1 0 0 1 0 0 1 <b2></b2>	C9	2	2	3
		CMP \$ zz	(A)–(M)		where	M=(zz)	0xxxxx00	1 1 0 0 0 1 0 1 <b2></b2>	C5	2	3	3
		CMP \$ zz, X	(A)–(M)	ize	where	M=(zz+(X))	0*****00	1 1 0 1 0 1 0 1 <b2></b2>	D5	2	4	3
		CMP \$ hhll	(A)–(M)	in s	where	M=(hhll)	Oxxxxx00	1 1 0 0 1 1 0 1 <b2></b2>	CD	3	4	3
		CMP \$ hhll, X	(A)–(M)	rison	where	M=(hhll+(X))	0xxxxx00	<b3> 1 1 0 1 1 1 0 1</b3>	DD	3	5	3
	uo	CMP \$ hhll, Y	(A)–(M)	ompa	where	M=(hhll+(Y))	0xxxxx00	<b2> <b3> 1 1 0 1 1 0 0 1</b3></b2>	D9	3	5	3
	aris	CMP (\$ zz. X)	(A)-(M)	ŏ	where	M=((77+(X)+1)(77+(X)))		<b2> <b3> 1 1 0 0 0 0 1</b3></b2>	C1	2	6	3
	dmo	CMP (\$ zz), Y	(A)–(M)	J	where	M = ((zz+1)(zz)+(Y))	0 * * * * * 00	<pre></pre>		2	6	3
	ŭ	0.001/ 11.0	(X)_nn			······································	0	<b2></b2>	=	-	2	
		CPX #\$nn	(X)_(M)	risor	where	M-(77)		<b2> 11100100</b2>		2	2	
		UPX \$ZZ	(X)_(M)	is is	where	M=(bbll)		<b2> 1110 1100</b2>			3	
		CPX \$ hhll		Jõ	WIICIC	······		<b2> <b3></b3></b2>	20	3	4	
		CPY #\$nn	(Y)–nn	son			0 x x x x x x 0 0	11000000 <b2></b2>	C0	2	2	
		CPY \$ zz	(Y)–(M)	npari	where	M=(zz)	$\circ$ xxxxx00	11000100 <b2></b2>	C4	2	3	
		CPY \$ hhll	(Y)–(M)	Con	where	M=(hhll)	0 x x x x x 0 0	1100 1100	CC	3	4	
				-			1	<b3></b3>	1	1		

RENESAS

Casestication         SYMBOL         FUNCTION         N V T B D I Z C         Drbubb D DDDrb HEX         NUMBER         N	Parameter Classification					INSTRUCTION CO	DDE	DE BYTE		
$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$			SYMBOL	FUNCTION	NVTBDIZC	D7D6D5D4 D3D2D1D0	HEX	NUMBER	NUMBER	NOTE
$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$			ASL A ASL \$zz	Left Shift [C]← <u>A7A6 A1A0</u> ← 0 where M=(zz)	0 x x x x x 00 0 x x x x x 00	0 0 0 0 1 0 1 0 0 0 0 0 0 1 1 0	0A 06	1 2	2 5	
$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$	1		ASL \$zz, X	where M=(zz+(X))	0 × × × × × 00	<b2> 0001 0110</b2>	16	2	6	
$ \begin{tabular}{ c c c c c c c c c c c c c c c c c c c$	1		ASL \$ hhll	C ← M7M6 M1M0 ← 0 where M=(hhII)	0xxxxx00	<b2> 0 0 0 0 1 1 1 0</b2>	0E	3	6	
$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$	1					<b2> <b3></b3></b2>		_		
$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$			ASL \$ hhll, X	J where M=(hhll+(X))	0 × × × × × 00	0 0 0 1 1 1 1 0 <b2> <b3></b3></b2>	1E	3	7	
$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$			LSR A LSR \$zz	Right Shift $0 \rightarrow \underline{A7A6  A1A0} \rightarrow \underline{C}$ where $M=(zz)$	0 × × × × × × 00 0 × × × × × 00	0 1 0 0 1 0 1 0 0 1 0 0 0 1 1 0	4A 46	1 2	2 5	
$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$			LSR \$zz, X	where $M=(zz+(X))$	0 × × × × × ○○	0101 0110	56	2	6	
$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$			LSR \$ hhll	$\begin{cases} \text{Right Shift 0} \rightarrow \boxed{\text{W1N0}} \rightarrow \text{W1N0$	0 × × × × × ○○	«В2» 0100_1110	4E	3	6	
$ \begin{array}{c c c c c c c c c c c c c c c c c c c $				where M. (bbll) (Y))		<b2> <b3></b3></b2>	55	2	7	
$ \begin{array}{c c c c c c c c c c c c c c c c c c c $	Į į		LSR \$ nnII, X	Since Wie(nnii+(X))		<pre></pre>	5E	3		
$\begin{array}{c c c c c c c c c c c c c c c c c c c $		ij	ROL A	Left Shift $\leftarrow \overline{A7A6}  A1A0 \leftarrow \overline{C} \leftarrow$	$0 \times \times \times \times \times 00$	< <u>B2&gt;</u> 0010 1010	2A	1	2	
$\begin{array}{c c c c c c c c c c c c c c c c c c c $	E	ۍ ا	ROL \$zz	where M=(zz)	0 × × × × × 00	0010 0110	26	2	5	
$\begin{array}{c c c c c c c c c c c c c c c c c c c $	atic	and	ROL \$zz, X	where M(zz+(X))	$0 \times \times \times \times \times 0$	<b2> 0 0 1 1 0 1 1 0</b2>	36	2	6	
$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$	Opera	te	- • •	Left Shift $\leftarrow M7M6 M1M0 \leftarrow C \leftarrow$		<b2></b2>				
$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$		ota	ROL \$ hhll	where M(hhII)	0xxxxx00	0010 1110 <b2></b2>	2E	3	6	
$\begin{array}{ c c c c c c c c c c c c c c c c c c c$		Υ.	ROL \$ hhll, X	where M(hhll+(X))	0×××××00	<b3> 0 0 1 1 1 1 1 0 <b2> <b3></b3></b2></b3>	ЗE	3	7	
$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$			ROR A	] Right Shift <sub>1</sub> → $C$ → $A7A6$ $A1A0$ <sub>1</sub> →	0xxxxx00	0110 1010	6A	1	2	
$\begin{array}{ c c c c c c c c } \hline ROR $zz, X \\ \hline RoR $hhll \\ \hline ROR $hll \\ $			ROR \$zz	where M=(zz)	0 × × × × × × 00	0110 0110	66	2	5	
ROR \$ hhll         where         M=(hhll)         O X X X X X O 0         0 1 1 0         1 1 1 0         6E         3         6			ROR \$zz, X	where M=(zz+(X)) Right Shift <sub>I</sub> →C → M7M6 M1M0 +	0×××××00	<b2> 0 1 1 1 0 1 1 0 <b2></b2></b2>	76	2	6	
			ROR \$ hhll	where M=(hhII)	0×××××00	0 1 1 0 1 1 1 0 <b2></b2>	6E	3	6	
ROR \$ hhll, X     where $M=(hhll+(X))$ $\bigcirc X \times X \times X \bigcirc \bigcirc$ $\bigcirc 1 \ 1 \ 1 \ 1 \ 1 \ 0 \ \langle B2 \rangle \\ \langle B2 \rangle \\ \langle B2 \rangle \rangle$ 7E     3     7			ROR \$ hhll, X	where M=(hhll+(X))	0 <b>x</b> x x x x x 00	<b3> 0 1 1 1 1 1 1 0 <b2> <b2></b2></b2></b3>	7E	3	7	
RRF \$ zz         M7         M4M3         M0         where         M=(zz)         X X X X X X X         1 0 0 0 0 0 1 0         82         2         8			RRF \$zz	M7 M4M3 M0 where M=(zz)	*****	1000 0010 <b2></b2>	82	2	8	
$\begin{array}{ c c c c c c c c c c c c c c c c c c c$		aut	CLB i, A	$(Ai) \leftarrow 0$ where i=0-7	******	iii1 1011	(1+2i)X10 +B	1	2	
$\begin{bmatrix} \mathbf{E} \\ \mathbf{E} \\ \mathbf{E} \\ \mathbf{E} \\ \mathbf{E} \\ \mathbf{C} \\ \mathbf{C} \\ \mathbf{C} \\ \mathbf{C} \\ \mathbf{K} \\ \mathbf{X} $	<u>+</u>	eme	CLB i, \$ zz	$(Mi) \leftarrow 0$ where i=0-7, M=(zz)	*****	iii1 1111	(1+2i)X10 +F	2	5	
Imon model     SEB i, A     (Ai) ←1     where     i=0-7     X X X X X X X X     i i i 0     1 0 1 1     2iX10     1     2	Ē	ag	SEB i, A	(Ai) ←1 where i=0—7	*****	<b2> iii0 1011</b2>	2i <b>X</b> 10	1	2	
$ \begin{array}{ c c c c c c c } \hline & & & & & & & & & & & & & & & & & & $		Mar	SEB i, \$ zz	$(Mi) \leftarrow 1$ where i=0-7, M=(zz)	*****	iii0 1111 <b2></b2>	+B 2ix10 +F	2	5	
CLC     (C) ← 0     X X X X X X 0     0 0 0 0 1     1 0 0 0     18     1     2			CLC	$(C) \leftarrow 0$	X X X X X X X 0	0001 1000	18	1	2	
SEC         (C) ← 1         X X X X X X 1         0 0 1 1         1 0 0 0         38         1         2			SEC	(C) ← 1	X X X X X X X 1	0011 1000	38	1	2	
$\square CLD \qquad (D) \leftarrow 0 \qquad \qquad X X X X 0 X X 1 1 0 1 1 0 0 0 D8 1 2$		-	CLD	$(D) \leftarrow 0$	x x x x 0 x x x	1101 1000	D8	1	2	
$\begin{array}{c c} & & & \\ \hline \\ \hline$			SED	(D) ← 1	x x x x 1 x x x	1111 1000	F8	1	2	
ion     CLI     (I) ← 0     X X X X 0 X X     0 1 0 1     1 0 0 0     58     1     2		se	CLI	(I) ← 0	x x x x x 0 x x	0101 1000	58	1	2	
B         SEI         (I) ←1         X X X X 1 X X         0 1 1 1         1 0 0 0         78         1         2		lag	SEI	(I) ← 1	x x x x x 1 x x	0111 1000	78	1	2	
LL     CLT $(T) \leftarrow 0$ $x \times 0 \times x \times x \times x$ $0 \ 0 \ 0 \ 1 \ 0 \ 0 \ 1 \ 0$ $12$ $1$ $2$		L	CLT	$0 \rightarrow (T)$	x x 0 x x x x x	0001 0010	12	1	2	
SET     (T) ← 1     X X 1 X X X X     0 0 1 1     0 0 1 0     32     1     2			SET	(T) ← 1	x x 1 x x x x x	0011 0010	32	1	2	
CLV         (V) ~ 0         X 0 X X X X X         1 0 1 1         1 0 0 0         B8         1         2			CLV	$(V) \leftarrow 0$	x 0 x x x x x x x	1011 1000	B8	1	2	

Parameter		0.445.01		FLAG	INSTRUCTION CC	DDE	BYTE	CYCLE	NOTE
Classi	ication	SYMBOL	FUNCTION	NVTBDIZC	D7D6D5D4 D3D2D1D0	HEX	NUMBER	NUMBER	NOTE
		BRA \$hhll	$(PC) \leftarrow (PC)+2+Rel$	* * * * * * * * *	1000 0000	80	2	4	4
	dmnr	JMP \$ hhll	(PC) ← hhll	* * * * * * * * *	0 1 0 0 1 1 0 0 <b2></b2>	4C	3	3	
		JMP (\$ hhll)	$(PCL) \leftarrow (hhII), \ (PCH) \leftarrow (hhII+1)$	* * * * * * * * *	0 1 1 0 1 1 0 0 <b2></b2>	6C	3	5	
		JMP (\$ zz)	$(PCL) \leftarrow (zz), \ (PCH) \leftarrow (zz+1)$	* * * * * * * * *	<b3> 1011 0010</b3>	B2	2	4	
		JSR \$ hhll	$\begin{array}{l} (M(S)) {\leftarrow} (PCH),  (S) {\leftarrow} (S) {-}1,  (M(S)) {\leftarrow}  (PCL), \\ (S) {\leftarrow} (S) {-}1,  \text{and}  (PC) {\leftarrow} \text{hhll} \end{array}$	* * * * * * * * *	<b2> 0 0 1 0 0 0 0 0 <b2></b2></b2>	20	3	6	
Branch and Return		JSR (\$ zz)	$\begin{array}{l} (M(S)) {\leftarrow} (PCH), \ (S) {\leftarrow} (S) - 1, \ (M(S)) {\leftarrow} (PCL), \\ (S) {\leftarrow} (S) - 1, \ (PCL) {\leftarrow} (zz), \ \text{and} \ (PCH) {\leftarrow} (zz{+}1) \end{array}$	*****	<b3> 0 0 0 0 0 0 1 0 <b2></b2></b3>	02	2	7	
		JSR \\$hhll	$\begin{array}{l} (M(S)) {\leftarrow} (PCH), \ (S) {\leftarrow} (S) {-} 1, \ (M(S)) {\leftarrow} (PCL), \\ (S) {\leftarrow} (S) {-} 1, \ (PCL) {\leftarrow} II, \ \text{ and } (PCH) {\leftarrow} FF \end{array}$	* * * * * * * * *	00100010 <b2></b2>	22	2	5	
		BBC i, A, \$ hhll	$ \begin{array}{llllllllllllllllllllllllllllllllllll$	****	iii1 0011 <b2></b2>	(1+2i)x10 +3	2	4	4
		BBC i, \$ zz, \$ hhll	$\begin{array}{llllllllllllllllllllllllllllllllllll$	* * * * * * * * *	iii1 0111 <b2></b2>	(1+2i)x10 +7	3	5	4
		BBS i, A, \$ hhll	$\begin{array}{lll} \mbox{When (Ai)=1} & (PC) \leftarrow (PC) + 2 + Rel & \mbox{Where} & i = 0 - 7 \\ \mbox{When (Ai)=0} & (PC) \leftarrow (PC) + 2 \end{array}$	* * * * * * * * *	iii0 0011 <b2></b2>	2ix10 +3	2	4	4
		BBS i, \$ zz, \$ hhll	$\begin{array}{llllllllllllllllllllllllllllllllllll$	*****	iii0 0111 <b2> <b3></b3></b2>	2ix10 +7	3	5	4
		BCC \$ hhll	$\begin{array}{lll} \mbox{When (C)=0} & (\mbox{PC}) \leftarrow (\mbox{PC}){+}2{+}\mbox{Rel} \\ \mbox{When (C)=1} & (\mbox{PC}) \leftarrow (\mbox{PC}){+}2 \end{array}$	*****	1001 0000 <b2></b2>	90	2	2	4
	Branch	BCS \$ hhll	$\begin{array}{lll} \mbox{When (C)=1} & (PC) \leftarrow (PC) + 2 + Rel \\ \mbox{When (C)=0} & (PC) \leftarrow (PC) + 2 \end{array}$	* * * * * * * * *	10110000 <b2></b2>	B0	2	2	4
		BNE \$ hhll	$ \begin{array}{ll} \mbox{When (Z)=0} & (PC) \leftarrow (PC) + 2 + Rel \\ \mbox{When (Z)=1} & (PC) \leftarrow (PC) + 2 \end{array} $	* * * * * * * * *	1 1 0 1 0 0 0 0 <b2></b2>	D0	2	2	4
		BEQ \$ hhll	$\begin{array}{lll} \mbox{When (Z)=1} & (\mbox{PC}) \leftarrow (\mbox{PC}) + 2 + \mbox{Rel} \\ \mbox{When (Z)=0} & (\mbox{PC}) \leftarrow (\mbox{PC}) + 2 \end{array}$	*****	1 1 1 1 0 0 0 0 <b2></b2>	F0	2	2	4
		BPL \$ hhll	$ \begin{array}{ll} \mbox{When (N)=0} & (PC) \leftarrow (PC) + 2 + Rel \\ \mbox{When (N)=1} & (PC) \leftarrow (PC) + 2 \end{array} $	*****	0001 0000 <b2></b2>	10	2	2	4
		BMI \$hhll	$ \begin{array}{ll} \mbox{When (N)=1} & (PC) \leftarrow (PC) + 2 + Rel \\ \mbox{When (N)=0} & (PC) \leftarrow (PC) + 2 \end{array} $	* * * * * * * * *	0 0 1 1 0 0 0 0 <b2></b2>	30	2	2	4
		BVC \$ hhll	$ \begin{array}{ll} \mbox{When (V)=0} & (PC) \leftarrow (PC) + 2 + Rel \\ \mbox{When (V)=1} & (PC) \leftarrow (PC) + 2 \end{array} $	*****	0101 0000 <b2></b2>	50	2	2	4
		BVS \$hhll	$ \begin{array}{ll} \mbox{When (V)=1} & (PC) \leftarrow (PC) + 2 + Rel \\ \mbox{When (V)=0} & (PC) \leftarrow (PC) + 2 \end{array} $	*****	01110000 <b2></b2>	70	2	2	4
	urn	RTI	$\begin{array}{l} (S) \leftarrow (S) + 1, \ (PS) \leftarrow (M(S)), \ (S) \leftarrow (S) + 1, \ (PCL) \leftarrow (M(S)), \\ (S) \leftarrow (S) + 1, \ and \ (PCH) \leftarrow (M(S)) \end{array}$	Previous status in stack	0100 0000	40	1	6	
	Ret	RTS	(S)←(S)+1, (PCL)←(M(S)), (S)←(S)+1, (PCH)←(M(S)), and (PC)←(PC)+1	****	0110 0000	60	1	6	
Inte	rrupt	BRK	$\begin{array}{l} (B) \leftarrow 1, \ (PC) \leftarrow (PC) + 2, \ (M(S)) \leftarrow (PCH), \ (S) \leftarrow (S) - 1, \ (M(S)) \leftarrow (PCL), \\ (S) \leftarrow (S) - 1, \ (M(S)) \leftarrow (PS), \ (S) \leftarrow (S) - 1, \ (I) \leftarrow 1, \ (PC) \leftarrow BADRS \end{array}$	X X X 1 X 1 X X	0000 0000	00	1	7	
Ot	her	NOP	(PC) ← (PC)+1	x x x x x x x x x	1110 1010	EA	1	2	
Spe	ecial	WIT	Internal clock source is stopped.	× × × × × × × × ×	1 1 0 0 0 0 1 0	C2	1	2	
		STP	Oscillation is stopped.	* * * * * * * * *	0100 0010	42	1	2	5

Symbol	Means	Symbol	Means
А	Accumulator	hh	High-order byte of address (0-255)
Ai	Bit i of accumulator	11	Low-order byte of address (0-255)
х	Index register X	zz	Zero page address (0—255)
Y	Index register Y	nn	Date at (0-255)
M	Memory	i	Data at (0-7)
Mi	Bit i of memory	iii	Data at (0-7)
PS	Processor status register	<b2></b2>	Second byte of instruction
S	Stack Pointer	<b3></b3>	Third byte of instruction
PC	Program counter	Rel	Relative address
PCL	Low-order byte of program counter	BADRS	Break address
РСн	High-order byte of program counter	←	Direction of data transfer
N	Negative flag	()	Contents of register of memory
V	Overflow flag	+	Add
Т	X modified operation mode flag	-	Subtract
В	Break flag	*	Multiplication
D	Decimal mode flag	÷	Division
I	Interrupt disable flag	~	Logical OR
Z	Zero flag	^	Logical AND
С	Carry flag	A	Logical Exclusive OR
#	Immediate mode	-	Negative
\$	Hexadecimal	X	Stable flag after execution
Ν.	Special page mode	0	Variable flag after execution

Notes 1: Listed function is when (T) = 0. When (T) = 1, (M(X)) is entered instead of (A) and the cycle number is increased by 3.
2: Ditto. The cycle number is increased by 2.
3: Ditto. The cycle number is increased by 1.
4: The cycle number is increased by 2 when a branch is occurred.
5: If the STP instruction is disabled the cycle number will be 2 (same in operation as two NOPs).

#### **APPENDIX 3. 740 Family list of Instruction Codes**

	D3 – D0	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
D7 – D4	Hexadecimal notation	0	1	2	3	4	5	6	7	8	9	A	В	С	D	E	F
0000	0	BRK	ORA IND, X	JSR ZP, IND	BBS 0, A	_	ORA ZP	ASL ZP	BBS 0, ZP	PHP	ORA IMM	ASL A	SEB 0, A	_	ORA ABS	ASL ABS	SEB 0, ZP
0001	1	BPL	ORA IND, Y	CLT	BBC 0, A	_	ORA ZP, X	ASL ZP, X	BBC 0, ZP	CLC	ORA ABS, Y	DEC A	CLB 0, A	_	ORA ABS, X	ASL ABS, X	CLB 0, ZP
0010	2	JSR ABS	AND IND, X	JSR SP	BBS 1, A	BIT ZP	AND ZP	ROL ZP	BBS 1, ZP	PLP	AND IMM	ROL A	SEB 1, A	BIT ABS	AND ABS	ROL ABS	SEB 1, ZP
0011	3	BMI	AND IND, Y	SET	BBC 1, A	_	AND ZP, X	ROL ZP, X	BBC 1, ZP	SEC	AND ABS, Y	INC A	CLB 1, A	LDM ZP	AND ABS, X	ROL ABS, X	CLB 1, ZP
0100	4	RTI	EOR IND, X	STP (Note)	BBS 2, A	COM ZP	EOR ZP	LSR ZP	BBS 2, ZP	РНА	EOR IMM	LSR A	SEB 2, A	JMP ABS	EOR ABS	LSR ABS	SEB 2, ZP
0101	5	BVC	EOR IND, Y	_	BBC 2, A	-	EOR ZP, X	LSR ZP, X	BBC 2, ZP	CLI	EOR ABS, Y	_	CLB 2, A	-	EOR ABS, X	LSR ABS, X	CLB 2, ZP
0110	6	RTS	ADC IND, X	MUL ZP, X (Note)	BBS 3, A	TST ZP	ADC ZP	ROR ZP	BBS 3, ZP	PLA	ADC IMM	ROR A	SEB 3, A	JMP IND	ADC ABS	ROR ABS	SEB 3, ZP
0111	7	BVS	ADC IND, Y	_	BBC 3, A	-	ADC ZP, X	ROR ZP, X	BBC 3, ZP	SEI	ADC ABS, Y	_	CLB 3, A	-	ADC ABS, X	ROR ABS, X	CLB 3, ZP
1000	8	BRA	STA IND, X	RRF ZP	BBS 4, A	STY ZP	STA ZP	STX ZP	BBS 4, ZP	DEY	-	ТХА	SEB 4, A	STY ABS	STA ABS	STX ABS	SEB 4, ZP
1001	9	BCC	STA IND, Y	_	BBC 4, A	STY ZP, X	STA ZP, X	STX ZP, Y	BBC 4, ZP	TYA	STA ABS, Y	TXS	CLB 4, A	_	STA ABS, X	_	CLB 4, ZP
1010	A	LDY IMM	LDA IND, X	LDX IMM	BBS 5, A	LDY ZP	LDA ZP	LDX ZP	BBS 5, ZP	TAY	LDA IMM	ТАХ	SEB 5, A	LDY ABS	LDA ABS	LDX ABS	SEB 5, ZP
1011	В	BCS	LDA IND, Y	JMP ZP, IND	BBC 5, A	LDY ZP, X	LDA ZP, X	LDX ZP, Y	BBC 5, ZP	CLV	LDA ABS, Y	TSX	CLB 5, A	LDY ABS, X	LDA ABS, X	LDX ABS, Y	CLB 5, ZP
1100	с	CPY IMM	CMP IND, X	WIT	BBS 6, A	CPY ZP	CMP ZP	DEC ZP	BBS 6, ZP	INY	CMP IMM	DEX	SEB 6, A	CPY ABS	CMP ABS	DEC ABS	SEB 6, ZP
1101	D	BNE	CMP IND, Y	_	BBC 6, A	_	CMP ZP, X	DEC ZP, X	BBC 6, ZP	CLD	CMP ABS, Y	_	CLB 6, A	-	CMP ABS, X	DEC ABS, X	CLB 6, ZP
1110	E	CPX IMM	SBC IND, X	DIV ZP, X (Note)	BBS 7, A	CPX ZP	SBC ZP	INC ZP	BBS 7, ZP	INX	SBC IMM	NOP	SEB 7, A	CPX ABS	SBC ABS	INC ABS	SEB 7, ZP
1111	F	BEQ	SBC	_	BBC 7, A	_	SBC ZP, X	INC ZP, X	BBC 7, ZP	SED	SBC ABS, Y	_	CLB 7, A	_	SBC ABS, X	INC ABS, X	CLB 7, ZP

Note: Some products unuse these instructions.

3-byte instruction

2-byte instruction

1-byte instruction

Refer to the related section because the clock control instruction and multiplication and division instruction depend on products. **MEMORANDUM** 

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# 740 Family Software Manual



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