COMMODORE SEMICONDUCTOR GROUP
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NMOS

6500/1 ONE-CHIP MICROCOMPUTER

INTRODUCTION

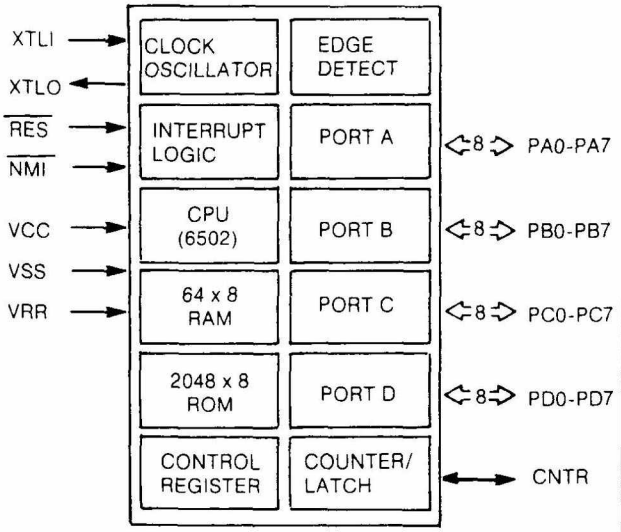
The 6500/1 is a complete, high-performance 8-bit NMOS microcomputer on a single chip, and is totally upward/downward software compatible with all members of the 6500 family.

The 6500/1 consists of a 6502 CPU, an internal clock oscillator, 2048 bytes of Read Only Memory (ROM), 64 bytes of Random Access Memory (RAM) and flexible interface circuitry. The interface circuitry includes a 16-bit programmable counter/latch with four operating modes, 32 bidirectional input/output lines (including two edge-sensitive lines), five interrupts and a counter I/O line.

FEATURES

- N-channel, silicon gate, depletion load technology
- 6502 CPU
  - —Software upward/downward compatibility
  - —Decimal or binary arithmetic modes
  - —13 addressing modes
  - —True direct and indirect indexing
  - —Memory addressable I/O
  - —Variable length stack
- 2048 x 8 mask programmable ROM
- 64 x 8 static RAM
- 32 bi-directional TTL compatible I/O lines (4 ports)
  - —1 positive edge sensitive line
  - —1 negative edge sensitive line
- 1 bi-directional TTL compatible counter I/O line with asynchronous operation in input mode
- 16-bit programmable counter/latch with four modes
  - —Interval Timer —Event Counter
  - —Pulse Generator —Pulse Width Measurement
- Five Interrupts
  - —Reset —Two external edge sensitive
  - —Non-maskable —Counter overflow
- 1 of 3 frequency references
  - —Crystal —Clock —RC (resistor only)
- 1 to 3 MHz internal clock frequency (available in 100KHz intervals). 6 MHz max crystal or clock external frequency.
- Single +5V power supply
- 1100 mW maximum operating power
- Separate power pin for RAM
- 40 pin DIP
- Compatible with R6500/1E Emulator

INTERFACE DIAGRAM



MASK PROGRAMMABLE OPTIONS

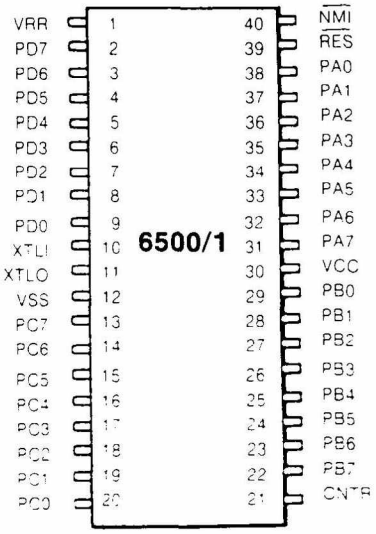
- Internal pull-up resistors on ports A, B, C, D. Selectable for 8-bit port groups only, not for individual port lines.
- Internal pull-up resistor on the CNTR line.

Note: The RC frequency option is available only in the 1 MHz 6500/1.

SIGNAL DESCRIPTIONS

Signal Name	Pin No.	Description
VCC	30	Main power supply + 5V
VRR	1	Separate power pin for RAM. In the event that VCC power is lost, this power retains RAM data.
VSS	12	Signal ground
XTLI	10	Crystal, clock or RC network input for internal clock oscillator.
XTLO	11	Crystal or RC network output from internal clock oscillator.
$\overline{RES}$	39	The Reset input is used to initialize the 6500/1. This signal must not transition from low to high for at least eight cycles after VCC reaches operating range and the internal oscillator has stabilized. + 10V input enables the test mode.
$\overline{NMI}$	40	A negative going edge on the Non-Maskable Interrupt signal requests that a non-maskable interrupt be generated within the CPU.
PA0-PA7 PB0-PB7 PC0-PC7 PD0-PD7	38-31 29-22 20-13 9-2	Four 8 bit ports used for either input/output. Each line consists of an active transistor to VSS and a passive pull-up to + 5V. The two lower bits of the PA port (PA0 and PA1) also serve as edge detect inputs with maskable interrupts.
CNTR	21	This line is used as a Counter input/output line. CNTR is an input in the Event Counter and Pulse Width Measurement modes and is an output in the Interval Timer and Pulse Generator modes.

PIN CONFIGURATION



FUNCTIONAL DESCRIPTION

This section gives a functional description of the logic blocks as shown in the block diagram.

CENTRAL PROCESSING UNIT (CPU)

Accumulator

The accumulator is a general purpose 8-bit register that stores the results of most arithmetic and logic operations. In addition, the accumulator usually contains one of the two data words used in these operations.

Index Registers

There are two 8-bit index registers, X and Y. These registers can be used for general purpose storage, or as a displacement to modify the base address and thus obtain a new effective address. Pre- or post-indexing of indirect addresses is possible.

Stack Pointer

The Stack Pointer is an 8-bit register. It is automatically incremented and decremented under control of the CPU to perform stack manipulation under direction of either the program or interrupts $\overline{NMI}$ and $\overline{IRQ}$. The stack allows simple implementation of nested subroutines and multiple level interrupts.

Arithmetic and Logic Unit (ALU)

All arithmetic and logic operations take place in the ALU, including incrementing and decrementing internal registers (except the Program Counter). The ALU cannot store data for more than one cycle. If data are placed on the inputs to the ALU at the beginning of a cycle, the result is always gated into one of the storage registers or to external memory during the next cycle.

Each bit of the ALU has two inputs. These inputs can be tied to various internal buses or to a logic zero; the ALU then generates the function (AND, OR, SUM, and so on) using the data on the two inputs.

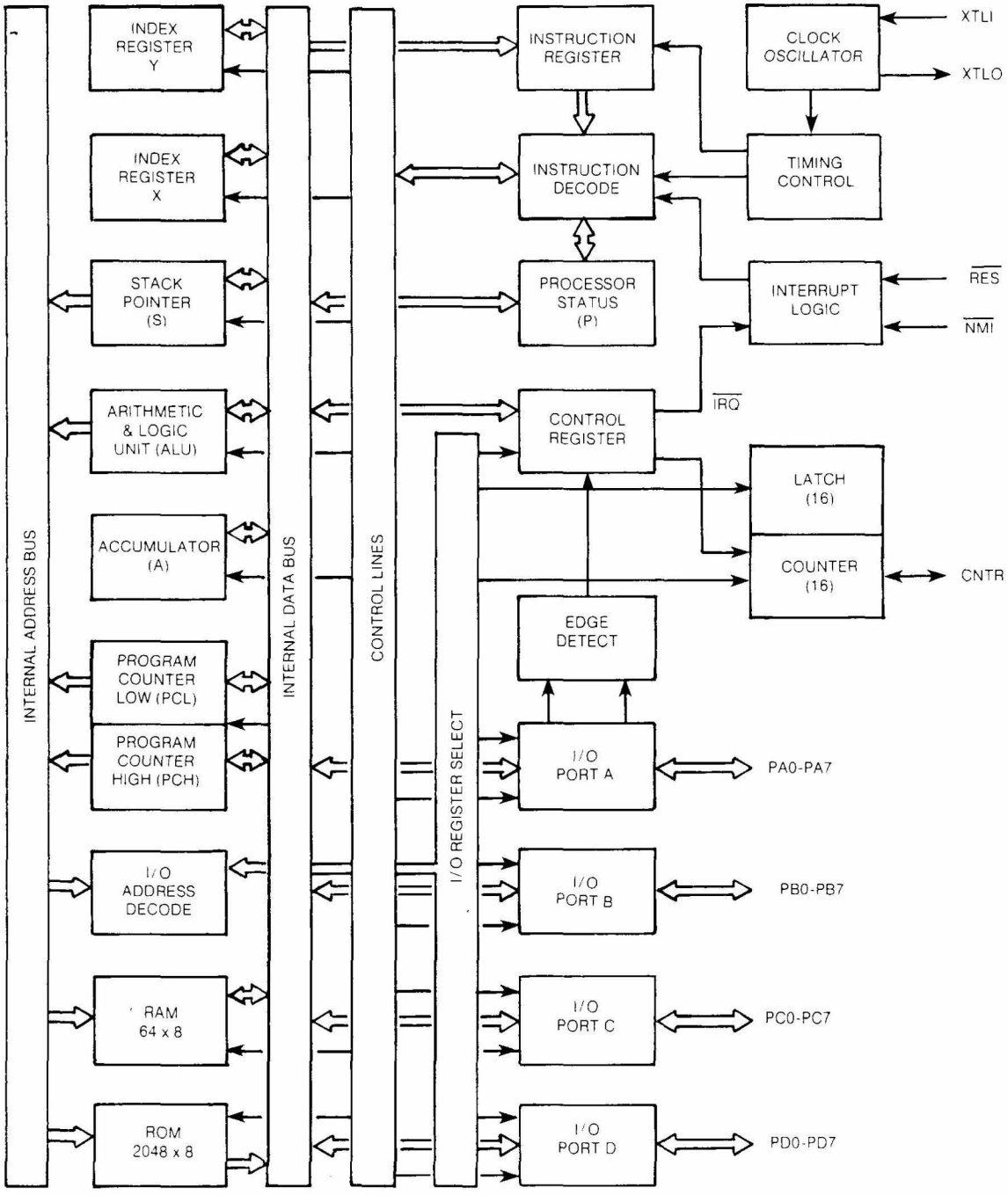
Timing Control

The Timing Control Logic keeps track of the specific instruction cycle being executed. Each data transfer which takes place between the registers is caused by decoding the contents of both the Instruction Register and Timing Control Logic.

Instruction Register and Decode

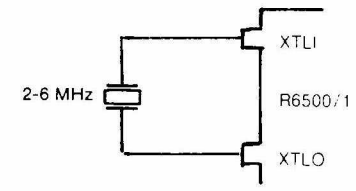
Instructions fetched from memory are gated onto the Internal Data Bus. These instructions are latched into the Instruction Register then deocoded, along with timing and interrupt signals, to generate control signals for the various registers.

6500/1 BLOCK DIAGRAM

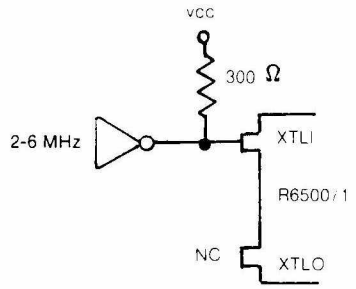


Clock Oscillator

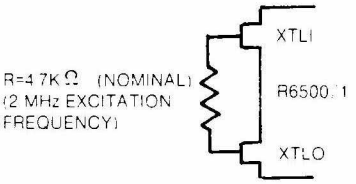
The Clock Oscillator provides the basic timing signals used by the 6500/1 CPU. The reference frequency is provided by an external source, and can be from a crystal, clock or RC network input. The RC network mode is a mask option. The external frequency can vary from 200 KHz to 6 MHz. The internal Phase 2 (Ø2) frequency is one-half the external reference frequency. A 4.7K ohm resistor will provide nominal 2 MHz oscillation and 1 MHz internal operation in the RC mask option (+ 35%).



a. Crystal Input



b. Clock Input



c. RC Network Input (Mask Option)

NOTE (1) C IS PROVIDED INTERNALLY BY THE R6500/1
(2) THE RC OPTION IS AVAILABLE ONLY ON THE 1 MHz R6500/1

Interrupt Logic

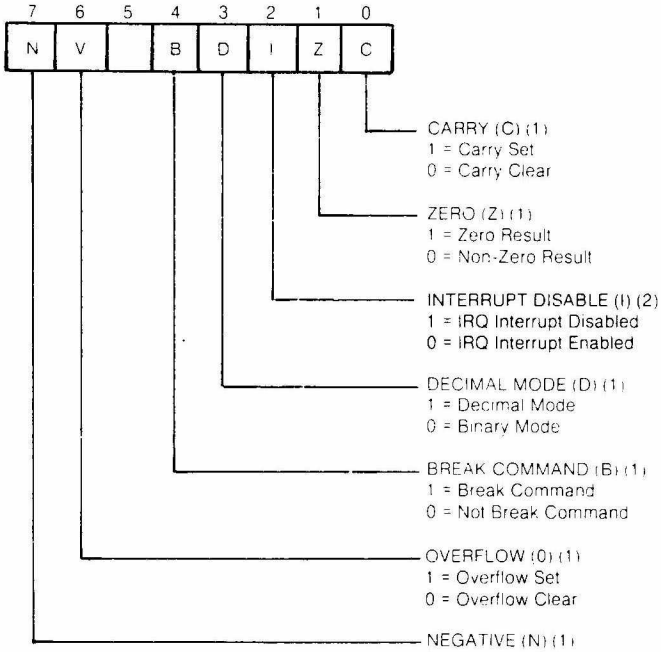
Interrupt logic controls the sequencing of three interrupts: $\overline{RES}$, $\overline{NMI}$ and $\overline{IRQ}$. $\overline{IRQ}$ is generated by any one of three conditions: Counter Overflow, PA0 Positive Edge Detected, and PA1 Negative Edge Detected. Multiple simultaneous interrupts on $\overline{IRQ}$ will cause the request to remain active until all interrupt conditions have been serviced and cleared.

Program Counter

The 16-bit Program Counter provides the addresses which step the CPU through sequential instructions in a program. The Program Counter is incremented each time an instruction or data is fetched from memory.

Processor Status Register

The 8-bit Processor Status Register contains seven status flags. Some of the flags are controlled by the program, others may be controlled both by the program and the CPU. The 6500 instruction set contains a number of conditional branch instructions which are designed to allow testing of these flags.



NOTES
(1) Not initialized by RES
(2) Set to Logic 1 by RES

Carry Bit (C)

The Carry Bit (C) can be considered as the ninth bit of an arithmetic operation. It is set to logic 1 if a carry from the eighth bit has occurred or cleared to logic 0 if no carry occurred as the result of arithmetic operations.

The Carry Bit may be set or cleared under program control by use of the Set Carry (SEC) or Clear Carry (CLC) instruction, respectively. Other operations which affect the Carry Bit are ADC, ASL, CMP, CPX, CPY, LSR, PLP, ROL, ROR, RTI, and SBC.

Zero Bit (Z)

The Zero Bit (Z) is set to logic 1 by the CPU during any data movement or calculation which sets all 8 bits of the result to zero. This bit is cleared to logic 0 when the resultant 8 bits of a data movement or calculation operation are not all zero. The 6500/1 instruction set

contains no instruction to specifically set or clear the Zero Bit. The Zero Bit is, however, affected by the following instructions: ADC, AND, ASL, BIT, CMP, CPX, CPY, DEC, DEX, DEY, EOR, INC, INX, INY, LDA, LDX, LDY, LSR, ORA, PLA, PLP, ROL, ROR, RTI, SBC, TAX, TAY, TXA, TSX, AND TYA.

Interrupt Disable Bit (I)

The Interrupt Disable Bit (I) is used to control the servicing of an interrupt request ($\overline{IRQ}$). If the I Bit is reset to logic 0, the $\overline{IRQ}$ signal will be serviced. If the bit is set to logic 1, the $\overline{IRQ}$ signal will be ignored. The CPU will set the Interrupt Disable Bit to logic 1 if a RESET ($\overline{RES}$) or Non-Maskable Interrupt ($\overline{NMI}$) signal is detected.

The I bit is cleared by the Clear Interrupt (CLI) instruction, the Pull Processor Status from Stack (PLP) instruction, or as the result of executing a Return from Interrupt (RTI) instruction (providing the Interrupt Disable Bit was cleared prior to the interrupt). The Interrupt Disable Bit may be set or cleared under program control using a Set Interrupt Disable (SEI) or a Clear Interrupt Disable (CLI) instruction, respectively.

Decimal Mode Bit (D)

The Decimal Mode Bit (D), is used to control the arithmetic mode of the CPU. When this bit is set to logic 1, the adder operates as a decimal adder. When this bit is cleared to logic 0, the adder operates as a straight binary adder. The adder mode is controlled only by the programmer. The Set Decimal Mode (SED) Instruction will set the D bit; the Clear Decimal Mode (CLD) Instruction will clear it. The PLP and RTI Instructions also effect the Decimal Mode Bit.

CAUTION

The Decimal Mode Bit will either set or clear in an unpredictable manner upon power application to R6500/1. This bit must be initialized to the desired state by the user program or erroneous results may occur.

Break Bit (B)

The Break Bit (B) is used to determine the condition which caused the $\overline{IRQ}$ service routine to be entered. If the $\overline{IRQ}$ service routine was entered because the CPU executed a BRK command, the Break Bit will be set to logic 1. If the $\overline{IRQ}$ routine was entered as the result of an $\overline{IRQ}$ signal being generated, the B bit will be cleared to logic 0. There are no instructions which can set or clear this bit.

Overflow Bit (V)

The Overflow Bit (V) is used to indicate that the result of a signed, binary addition, or subtraction, operation is a value that cannot be contained in seven bits (-128 n 127). This indicator only has meaning when signed arithmetic (sign and seven magnitude bits) is performed. When the ADC or SBC instruction is performed, the Overflow Bit is set to logic 1 if the polarity of the sign bit (bit 7) is changed because the result exceeds + 127 or -128; otherwise the bit is cleared to logic 0. The V bit may also be cleared by the programmer using a Clear Overflow (CLV) instruction.

The Overflow Bit may also be used with the BIT Instruction. The BIT Instruction which may be used to sample interface devices, allows the overflow flag to reflect the condition of bit 6 in the sampled field. During a BIT Instruction the Overflow Bit is set equal to the content of the bit 6 on the data tested with BIT Instruction. When used in this mode, the overflow has nothing to do with signed arithmetic, but is just another sense bit for the microprocessor. Instructions which affect the V flag are ADC, BIT, CLV, PLP, RTI and SBC.

Negative Bit (N)

The Negative Bit (N) is used to indicate that the sign bit (bit 7), in the resulting value of a data movement or data arithmetic operation, is set to logic 1. If the sign bit is set to logic 1, the resulting value of the data movement or arithmetic operation is negative; if the sign bit is cleared, the result of the data movement or arithmetic operation is positive. There are no instructions that set or clear the Negative Bit since the Negative Bit represents only the status of a result. The Instructions that effect the state of the Negative Bit are: ADC, AND, ASL, BIT, CMP, CPX, CPY, DEC, DEX, DEY, EOR, INC, INX, INY, LDA, LDX, LDY, LSR, ORA, PLA, PLP, ROL, ROR, RTI, SBC, TAX, TAY, TSX, TXA, and TYA.

MEMORY

2048 x 8 ROM

The 2048 byte Read-Only Memory (ROM) contains the program instructions and other fixed constants. These program instructions and constants are mask programmed into the ROM during fabrication of the 6500/1 device. The 6500/1 ROM is memory mapped from 800 to FFF.

64 x 8 RAM

The 64 byte Random Access Memory (RAM) is used for read/write memory during system operation, and contains the stack. This RAM is completely static in operation and requires no clock or dynamic refresh. A standby power pin, VRR, allows RAM memory to be maintained on 10% of the operating power in the event that VCC power is lost.

In order to take advantage of efficient zero page addressing capabilities, the RAM is assigned memory addresses 0 to 03F.

INPUT/OUTPUT

Bidirectional I/O Ports

The 6500/1 provides four 8-bit input/output ports (PA, PB, PC, and PD). Associated with the I/O ports are four 8-bit registers located on page zero. See the system memory map for specific addresses. Each I/O line is individually selectable as an input or an output without line grouping or port association restrictions.

An internal active transistor drives each I/O line to the low state. An internal passive resistance pulls the I/O lines to the high state, eliminating the need for external pull-up resistors.

An option is available to delete the internal pull-up resistance on 8-bit port groups or on the CNTR line at mask time. This option is employed to permanently assign an 8-bit port group to input functions, to interface with CMOS drivers, or to interface with external pull-up devices.

Inputs

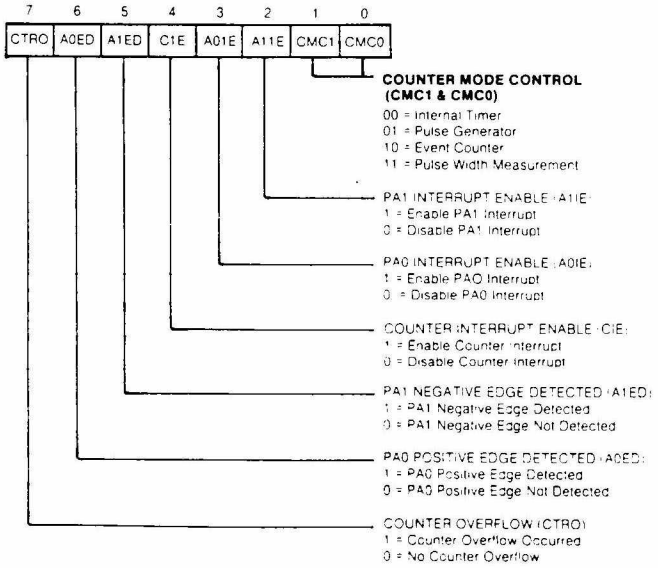
Inputs are enabled by setting the appropriate bit of the I/O port to the high state (Logic 1). A low input signal causes a logic 0 to be read. A high input signal causes a logic 1 to be read. $\overline{RES}$ loads Logic 1 into the I/O ports, thereby initializing all I/O lines as inputs.

Outputs

Outputs are set by loading the desired bit pattern into corresponding I/O ports. A Logic 1 selects a high output; a Logic 0 selects a low output.

CONTROL REGISTER

The Control Register (CR), located at address 08F, controls four Counter operating modes and three maskable interrupts. It also reports the status of three interrupt conditions. There are five control bits and three status bits. The control bits are set to Logic 1 or cleared to Logic 0 by writing the desired state into the respective bit positions. The Control Register is cleared to Logic 0 by the occurrence of $\overline{RES}$.



EDGE DETECT CAPABILITY

There is an asynchronous edge detect capability on two of the Port A I/O lines. This capability exists in addition to and independently from the normal Port A I/O functions. The maximum rate at which an edge can be detected is one-half the Ø2 clock rate. The edge detect logic is continuously active. Each edge detect signal is associated with a maskable interrupt.

PA0 Positive Edge Detection

A positive (rising) edge is detectable on PA0. When this edge is detected, the PA0 Positive Edge Detected bit—Bit 6 in the Control Register—is set to Logic 1. When both this bit and the PA0 Interrupt Enable Bit—Bit 3 of the Control Register—are set to Logic 1, an $\overline{IRQ}$ interrupt request is generated. The PA0 Positive Edge Detected bit is cleared by writing to address 089.

The edge detecting circuitry is active when PA0 is used either as an input or as an output. When PA0 is used as an output, A0ED will be set when the positive edge is detected during a logical 0 to 1 transition.

When PA0 is used as an input and the positive edge detecting circuitry is used, A0ED should be cleared by the user program upon initialization and upon completion of PA0 Positive Edge Detected $\overline{IRQ}$ processing.

PA1 Negative Edge Detection

A negative (falling) edge is detectable on PA1. When this edge is detected, the PA1 Negative Edge Detected bit—Bit 5 of the Control Register—is set to Logic 1. When both this bit and the PA1 Interrupt Enable bit—Bit 2 of the Control Register—are set to Logic 1, an $\overline{IRQ}$ interrupt request is generated. The PA1 Negative Edge Detected bit is cleared by writing to address 08A.

The edge detecting circuitry is active when PA1 is used either as an input or as an output. When PA1 is used as an output, A1ED will be set when the negative edge is detected during a logical 1 to 0 transition.

When PA1 is used as an Input and the negative edge detecting circuitry is used, A1ED should be cleared by the user program upon initialization and when the PA1 Negative Edge Detected $\overline{IRQ}$ processing is completed.

COUNTER/LATCH

The Counter/Latch consists of a 16-bit decrementing Counter and a 16-bit Latch. The Counter is comprised of two 8-bit registers. Address 086 contains the Upper Count (UC) and address 087 contains the Lower Count (LC). The Counter counts either Ø2 clock periods or occurrences of an external event, depending on the selected counter mode. The UC and LC can be read at any time without affecting counter operation.

The Latch contains the Counter preset value. The Latch consists of two 8-bit registers. Address 084 contains the Upper Latch (UL) and address 085 contains the lower latch (LL). The 16-bit Latch can hold a count from 0 to 65,535. The Latch can be accessed as two write-only memory locations.

The Latch registers can be loaded at any time by storing into UL and LL. The UL can also be loaded by writing into address 088.

The Counter can be preset at any time by writing to address 088. Presetting the Counter in this manner causes the contents of the accumulator to be stored into the UL before the 16-bit value in the Latch (UL and LL) is transferred in the Counter (UC and LC).

The Counter is preset to the Latch value when the Counter overflows. When the counter decrements from 0000, Counter overflow occurs causing the next counter value to be the Latch value, not FFFF.

When the Counter overflows, Counter Overflow bit—Bit 7 of the Control Register—is set to Logic 1. When both this bit and the Counter Interrupt Enable bit—Bit 4 of the Control Register—are set, an $\overline{IRQ}$ interrupt request is generated. The Counter Overflow bit in the Control Register can be examined in an $\overline{IRQ}$ interrupt service routine to determine that the $\overline{IRQ}$ was generated by Counter overflow.

COUNTER OVERFLOW

The Counter Overflow Bit is set to Logic 1 whenever a counter overflow occurs in any of the four counter operating modes. Overflow occurs when the counter is decremented one count from 0000. This bit is cleared to logic 0 by $\overline{RES}$ or by reading from address 087 or writing to address 088.

This bit should be cleared by the user program upon initialization and upon completion of Counter Overflow $\overline{IRQ}$ interrupt processing.

When a Counter Overflow occurs, the Upper Count (UC) in address 086 and the Lower Count (LC) in address 087 are reset to the values contained in the Upper Latch (UL) in address 084 and in the Lower Latch (LL) in address 085, respectively. Therefore, it is important to load the Lower Latch value prior to executing the Write to Upper Latch and Transfer Latch to Counter (address 088) in order to prevent an unpredicted reoccurrence of Counter Overflow and, if enabled, an $\overline{IRQ}$ interrupt request.

COUNTER MODES

The Counter operates in any of four modes. These modes are selected by the Counter Mode Control bits in the Control Register.

Mode	CMC 1	CMC 0
Interval Timer	0	0
Pulse Generator	0	1
Event Counter	1	0
Pulse Width Measurement	1	1

The Interval Timer, Pulse Generator, and Pulse Width Measurement Modes are Ø2 clock counter modes. The Event Counter Mode counts the occurrences of an external event on the CNTR line.

Interval Timer (Mode 0)

In this mode the Counter is free running and decrements at the Ø2 clock rate. Counter overflow sets the Control Register status bit and causes the Counter to be preset to the Latch value. The Counter is also preset to the latch value by performing a write operation to counter address 088.

The Counter value is decremented by one count at the Ø2 clock rate. The 16-bit Counter can hold from 1 to 65535 counts. The Counter Timer capacity is therefore 1 us to 65.535ms at the 1 MHz Ø2 clock rate or 0.5 us to 32.768ms at the 2 MHz Ø2 clock rate. Time intervals greater than the maximum Counter value can be easily measured by counting $\overline{IRQ}$ interrupt requests in the counter $\overline{IRQ}$ interrupt routine.

While operated in this mode, the CNTR line is held in the high state.

Pulse Generator (Mode 1)

In this mode the Counter is free running and decrements at the Ø2 clock rate. The Counter Out/Event In line (CNTR) operates as Counter Out. Counter overflow sets the Control Register status bit and causes the Counter to be preset to the Latch value.

The CNTR line toggles from one state to the other when Counter overflow occurs. Writing to address 088 will also toggle the CNTR line.

A symmetric or asymmetic output waveform can be generated on the CNTR line in this mode. A one-shot waveform can easily be generated by changing from Mode 1 to Mode 0 after only one occurrence of the output toggle condition.

Event Counter (Mode 2)

In this mode the CNTR line is used as an event input line. The Counter decrements each time a rising edge is detected on CNTR. The maximum rate at which this edge can be detected is one-half the Ø2 clock rate. Counter overflow sets the Control Register status bit and causes the Counter to be preset to the Latch value.

External events on the CNTR line may be fully asynchronous to the 6500/1 clock.

Pulse Width Measurement (Mode 3)

This mode allows the accurate measurement of the duration of a low state on the CNTR line. The Counter decrements at the Ø2 clock rate as long as the CNTR line is held in the low state. The Counter is stopped when CNTR is in the high state. If the CNTR pin is left disconnected, this mode may be selected to stop the Counter since the internal pull-up device will cause the CNTR input to be in the high state.

RESET CONSIDERATIONS

The occurrence of $\overline{RES}$ going from low to high causes initialization of various conditions in the 6500/1. All of the I/O ports (PA, PB, PC, and PD) and CNTR are forced to the high (Logic 1) state. All bits of the Control Register are reset to Logic 0, causing the Interval Timer Mode (Mode 0) to be selected and all interrupt enabled bits to be cleared. Neither the Latch nor the Counter registers are initialized by $\overline{RES}$. The Interrupt Disable bit in the CPU Processor Status Register is set and the program starts execution at the address contained in the Reset Vector location.

POWER ON/OFF TIMING

After application of VCC power to the R6500/1, $\overline{RES}$ must be held low for at least eight Ø2 clock cycles after VCC reaches operating range and the internal clock oscillator has stabilized. This stabilization time is dependent upon the input VCC voltage and performance of the crystal, clock, or RC network input circuit. The clock oscillator output can be monitored on XTLO (pin 11).

RAM DATA RETENTION—VRR REQUIREMENTS

For the RAM to retain data upon loss of VCC, VRR must be supplied within operating range and $\overline{RES}$ must be driven low at least eight Ø2 clock pulses before VCC falls out of operating range. $\overline{RES}$ must then be held low while VCC is out of operating range and until at least eight Ø2 clock cycles after VCC is again within operating range and the internal Ø2 oscillator is stabilized. VRR must remain within VCC operation range during normal R6500/1 operation. When VCC is out of operating range, VRR must remain within the VRR retention range in order to retain data.

TEST LOGIC

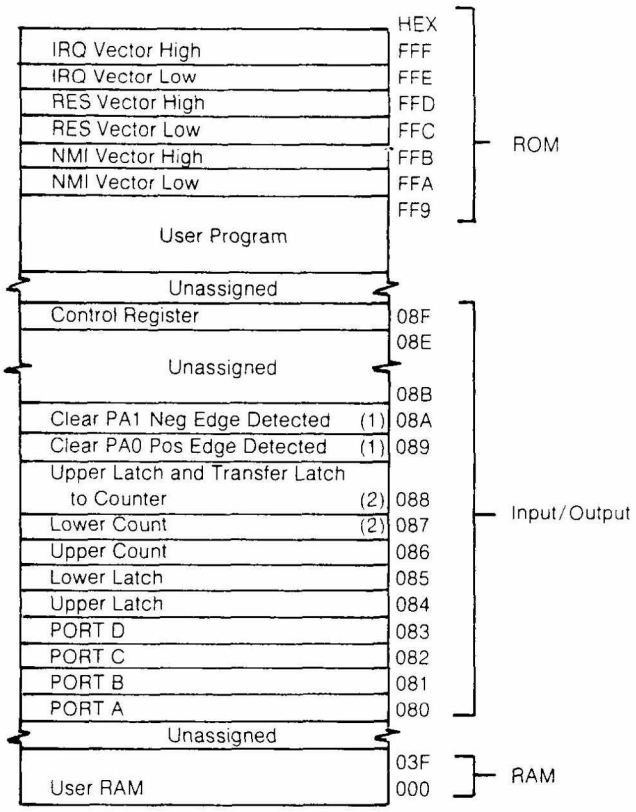
Special test logic provides a method for thoroughly testing the 6500/1. Applying a +10V signal to the $\overline{RES}$ line places the 6500/1 in the test mode. While in this mode, all memory fetches are made from Port PC. External test equipment can use this feature to test internal CPU logic and I/O. A program can be loaded into RAM allowing the contents of the instruction ROM to be dumped to any port for external verification.

All 6500/1 microcomputers are tested by Commodore Semiconductor Group using this feature.

MEMORY ADDRESSABLE I/O

The I/O ports, registers, and commands are treated as memory and are assigned specific addresses. See the system memory map for the addresses. This I/O technique allows the full set of CPU instructions to be used in the generation and sampling of I/O commands and data. When an instruction is executed with an I/O address and appropriate R/W state, the corresponding I/O function is performed.

SYSTEM MEMORY MAP



Notes:
(1) I/O command only; i.e., no stored data.
(2) Clears Counter Overflow—Bit 7 in Control Register.

ADDRESSING MODES

Accumulator Addressing

This form of addressing is represented with a one byte instruction, implying an operation on the accumulator.

Immediate Addressing

In immediate addressing, the operand is contained in the second byte of the instruction, with no further memory addressing required.

Absolute Addressing

In absolute addressing, the second byte of the instruction specified the eight low order bits of the effective address while the third byte specifies the eight high order bits. Thus, the absolute addressing mode allows access to the entire 65K bytes of addressable memory.

Zero Page Addressing

The zero page instructions allow for shorter code and execution times by only fetching the second byte of the instruction and assuming a zero high address byte. Careful use of the zero page can result in significant increase in code efficiency.

Indexed Zero Page Addressing

(X, Y indexing). This form of addressing is used in conjunction with the index register and is referred to as "Zero Page, X" or "Zero Page, Y." The effective address is calculated by adding the second byte to the contents of the index register. Since this is a form of "Zero Page" addressing, the content of the second byte references a location in page zero. Additionally, due to the "Zero Page" addressing nature of this mode, no carry is added to the high order 8 bits of memory and crossing of page boundaries does not occur.

Indexed Absolute Addressing

(X, Y indexing). This form of addressing is used in conjunction with X and Y index register and is referred to as "Absolute, X," and "Absolute, Y." The effective address is formed by adding the contents of X and Y to the address contained in the second and third bytes of the instruction. This mode allows the index register to contain the index or count value and the instruction to contain the base address. This type of indexing allows any location referencing and the index to modify multiple fields resulting in reduced coding and execution time.

Implied Addressing

In the implied addressing mode, the address containing the operand is implicitly stated in the operation code of the instruction.

Relative Addressing

Relative addressing is used only with branch instructions and establishes a destination for the conditional branch.

The second byte of the instruction becomes the operand which is an "Offset" added to the contents of the lower eight bits of the program counter when the counter is set at the next instruction. The range of the offset is -128 to +127 bytes from the next instruction.

Indexed Indirect Addressing

In indexed indirect addressing (referred to as [Indirect, X]), the second byte of the instruction is added to the contents of the X index register, discarding the carry. The result of this addition points to a memory location on page zero whose contents is the low order eight bits of the effective address. The next memory location in page zero contains the high order eight bits of the effective address. Both memory locations specifying the high and low order bytes of the effective address must be in page zero.

Indirect Indexed Addressing

In indirect indexed addressing (referred to as [Indirect, Y]), the second byte of the instruction points to a memory location in page zero. The contents of this memory location is added to the contents of the Y index register, the result being the low order eight bits of the effective address. The carry from this addition is added to the contents of the next page zero memory location, the result being the high order eight bits of the effective address.

Absolute Indirect

The second byte of the instruction contains the low order eight bits of a memory location. The high order eight bits of that memory location is contained in the third byte of the instruction. The contents of the fully specified memory location is the low order byte of the effective address. The next memory location contains the high order byte of the effective address which is loaded into the sixteen bits of the program counter.

INSTRUCTION SET—ALPHABETIC SEQUENCE

ADC	Add Memory to Accumulator with Carry
AND	"AND" Memory with Accumulator
ASL	Shift Left One Bit (Memory or Accumulator)
BCC	Branch on Carry Clear
BCS	Branch on Carry Set
BEQ	Branch on Result Zero
BIT	Test Bits in Memory with Accumulator
BMI	Branch on Result Minus
BNE	Branch on Result not Zero
BPL	Branch on Result Plus
BRK	Force Break
BVC	Branch on Overflow Clear
BVS	Branch on Overflow Set
CLC	Clear Carry Flag
CLD	Clear Decimal Mode
CLI	Clear Interrupt Disable Bit
CLV	Clear Overflow Flag
CMP	Compare Memory and Accumulator
CPX	Compare Memory and Index X
CPY	Compare Memory and Index Y
DEC	Decrement Memory by One
DEX	Decrement Index X by One
DEY	Decrement Index Y by One
EOR	"Exclusive-or" Memory with Accumulator
INC	Increment Memory by One
INX	Increment Index X by One
INY	Increment Index Y by One
JMP	Jump to New Location
JSR	Jump to New Location Saving Return Address
LDA	Load Accumulator with Memory
LDX	Load Index X with Memory
LDY	Load Index Y with Memory
LSR	Shift One Bit Right (Memory or Accumulator)
NOP	No Operation
ORA	"OR" Memory with Accumulator
PHA	Push Accumulator on Stack
PHP	Push Processor Status on Stack
PLA	Pull Accumulator from Stack
PLP	Pull Processor Status from Stack
ROL	Rotate One Bit Left (Memory or Accumulator)
ROR	Rotate One Bit Right (Memory or Accumulator)
RTI	Return from Interrupt
RTS	Return from Subroutine
SBC	Subtract Memory from Accumulator with Borrow
SEC	Set Carry Flag
SED	Set Decimal Mode
SEI	Set Interrupt Disable Status
STA	Store Accumulator in Memory
STX	Store Index X in Memory
STY	Store Index Y in Memory
TAX	Transfer Accumulator to Index X
TAY	Transfer Accumulator to Index Y
TSX	Transfer Stack Pointer to Index X
TXA	Transfer Index X to Accumulator
TXS	Transfer Index X to Stack Register
TYA	Transfer Index Y to Accumulator

INSTRUCTION SET

INSTRUCTION SET—OP CODES, Execution Time, Memory Requirements

INSTRUCTIONS				IMMEDIATE			ABSOLUTE			ZERO PAGE			ACCUM.			IMPLIED			(IND, X)			(IND), Y			Z. PAGE, X			ABS. X			ABS. Y			RELATIVE			INDIRECT			Z. PAGE, Y			CONDITION CODES					
MNEMONIC			OPERATION	OP	N	#	OP	N	#	OP	N	#	OP	N	#	OP	N	#	OP	N	#	OP	N	#	OP	N	#	OP	N	#	OP	N	#	OP	N	#	OP	N	#	OP	N	#	N	Z	C	I	D	V
A	D	C	A + M + C → A	(1) (4)	69	2	2	6D	4	3	65	3	2							61	6	2	71	5	2	75	4	2	7D	4	3	79	4	3														
A	N	D	A ∧ M → A	(1)	29	2	2	2D	4	3	25	3	2							21	6	2	31	5	2	35	4	2	3D	4	3	39	4	3														
A	S	L	C ← [7 0] ← Ø					0E	6	3	06	5	2	0A	2	1										16	6	2	1E	7	3															
B	C	C	BRANCH ON C = Ø	(2)																															90	2	2											
B	C	S	BRANCH ON C = 1	(2)																															B0	2	2											
B	E	Q	BRANCH ON Z = 1	(2)																															F0	2	2											
B	I	T	A ∧ M					2C	4	3	24	3	2																													M7	↕	–	–	–	M6
B	M	I	BRANCH ON N = 1	(2)																															30	2	2											
B	N	E	BRANCH ON Z = Ø	(2)																															D0	2	2											
B	P	L	BRANCH ON N = Ø	(2)																															10	2	2											
B	R	K														00	7	1																													
B	V	C	BRANCH ON V = Ø	(2)																															50	2	2											
B	V	S	BRANCH ON V = 1	(2)																															70	2	2											
C	L	C	Ø → C													18	2	1																													
C	L	D	Ø → D													D8	2	1																													
C	L	I	Ø → I													58	2	1																													
C	L	V	Ø → V													B8	2	1																													
C	M	P	A – M	(1)	C9	2	2	CD	4	3	C5	3	2							C1	6	2	D1	5	2	D5	4	2	DD	4	3	D9	4	3														
C	P	X	X – M		E0	2	2	EC	4	3	E4	3	2																																		
C	P	Y	Y – M		C0	2	2	CC	4	3	C4	3	2																																		
D	E	C	M – 1 → M					CE	6	3	C6	5	2													D6	6	2	DE	7	3															
D	E	X	X – 1 → X													CA	2	1																												
D	E	Y	Y – 1 → Y													88	2	1																												
E	O	R	A ⊻ M → A	(1)	49	2	2	4D	4	3	45	3	2							41	6	2	51	5	2	55	4	2	5D	4	3	59	4	3														
I	N	C	M + 1 → M					EE	6	3	E6	5	2													F6	6	2	FE	7	3															
I	N	X	X + 1 → X													E8	2	1																												
I	N	Y	Y + 1 → Y													C8	2	1																												
J	M	P	JUMP TO NEW LOC					4C	3	3																									6C	5	3											
J	S	R	JUMP SUB					20	6	3																																				
L	D	A	M → A		A9	2	2	AD	4	3	A5	3	2							A1	6	2	B1	5	2	B5	4	2	BD	4	3	B9	4	3														

MNEMONIC			OPERATION	IMMEDIATE			ABSOLUTE			ZERO PAGE			ACCUM.			IMPLIED			(IND, X)			(IND), Y			Z. PAGE, X			ABS. X			ABS. Y			RELATIVE			INDIRECT			Z. PAGE, Y			CONDITION CODES					
				OP	N	#	OP	N	#	OP	N	#	OP	N	#	OP	N	#	OP	N	#	OP	N	#	OP	N	#	OP	N	#	OP	N	#	OP	N	#	OP	N	#	OP	N	#	N	Z	C	I	D	V
L	D	X	M → X		A2	2	2	AE	4	3	A6	3	2													B6	4	2													E6	4	2						
L	D	Y	M → Y		A0	2	2	AC	4	3	A4	3	2													B4	4	2	BC	4	3																	
L	S	R	Ø → [7 0] → C					4E	6	3	46	5	2	4A	2	1										56	6	2	5E	7	3																	
N	O	P	NO OPERATION													EA	2	1																													
O	R	A	A ∨ M → A		09	2	2	0D	4	3	05	3	2							01	6	2	11	5	2	15	4	2	1D	4	3	19	4	3														
P	H	A	A → M(S)	S – 1 → S												48	3	1																													
P	H	P	P → M(S)	S – 1 → S												08	3	1																													
P	L	A	S + 1 → S	M(S) → A												68	4	1																													
P	L	P	S + 1 → S	M(S) → P												28	4	1																												(RESTORED)		
R	O	L	[7 0] ← C					2E	6	3	26	5	2	2A	2	1										36	6	2	3E	7	3															
R	O	R	C → [7 0]					6E	6	3	66	5	2	6A	2	1										76	6	2	7E	7	3															
R	T	I	RTRN INT													40	6	1																												(RESTORED)		
R	T	S	RTRN SUB													60	6	1																													
S	B	C	A – M – C → A	(1)	E9	2	2	ED	4	3	E5	3	2							E1	6	2	F1	5	2	F5	4	2	FD	4	3	F9	4	3											(3)			
S	E	C	1 → C													38	2	1																													
S	E	D	1 → D													F8	2	1																													
S	E	I	1 → I													78	2	1																													
S	T	A	A → M					8D	4	3	85	3	2							81	6	2	91	6	2	95	4	2	9D	5	3	99	5	3														
S	T	X	X → M					8E	4	3	86	3	2																													96	4	2						
S	T	Y	Y → M					8C	4	3	84	3	2													94	4	2																			
T	A	X	A → X													AA	2	1																													
T	A	Y	A → Y													A8	2	1																													
T	S	X	S → X													BA	2	1																													
T	X	A	X → A													8A	2	1																													
T	X	S	X → S													9A	2	1																													
T	Y	A	Y → A													98	2	1																													

(1) ADD 1 TO "N" IF PAGE BOUNDRY IS CROSSED
(2) ADD 1 TO "N" IF BRANCH OCCURS TO SAME PAGE
ADD 2 TO "N" IF BRANCH OCCURS TO DIFFERENT PAGE
(3) CARRY NOT–BORROW
(4) IF IN DECIMAL MODE Z FLAG IS INVALID
ACCUMULATOR MUST BE CHECKED FOR ZERO RESULT

X INDEX X
Y INDEX Y
A ACCUMULATOR
M MEMORY PER EFFECTIVE ADDRESS
M(S) MEMORY PER STACK POINTER

+ ADD
– SUBTRACT
∧ AND
∨ OR
⊻ EXCLUSIVE OR
↕ MODIFIED
– NOT MODIFIED
M7 MEMORY BIT 7
M6 MEMORY BIT 6

N NO. CYCLES
NO. BYTES

Note: Commodore Semiconductor Group cannot assume liability for the use of undefined OP Codes

SPECIFICATIONS

Maximum Ratings

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	-.0.3 to +7.0	Vdc
Input Voltage	V_{in}	-.03 to +7.0	Vdc
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	-55 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages, however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this circuit.

STATIC D.C. CHARACTERISTICS (V_{CC} = 5V + 5%, T_A = 0° -70° C)

Characteristic	Symbol	Min	Typ	Max	Unit
Power Dissipation (Outputs High)	P_D	—	500	1100	mW
RAM Standby Voltage (Retention Mode)	V_{RR}	3.5	—	V_{CC}	Vdc
RAM Standby Current (Retention Mode)	I_{RR}	—	10	—	mAdc
Input High Voltage (Normal Operating Levels)	V_{IH}	+2.0	—	V_{CC}	Vdc
Input Low Voltage (Normal Operating Levels)	V_{IL}	-0.3	—	+0.8	Vdc
Input Leakage Current					
V_{in} = 0 to 5.0 Vdc	I_{IN}	—	±1.0	±2.5	μAdc
RES, NMI		—	±1.0	—	μAdc
Input High Voltage (XTLI)	V_{IHXT}	+4.0	—	V_{CC}	Vdc
Input Low Voltage (XTLI)	V_{ILXT}	-0.3	—	+0.8	Vdc
Input Low Current					
(V_{IL} = 0.4 Vdc)	I_{IL}	—	-1.0	-1.6	mAdc
Output High Voltage					
(V_{CC} = min, I_{Load} = -100 μAdc)	V_{OH}	2.4	—	—	Vdc
Output High Voltage					
(V_{CC} = min)	V_{CMOS}	V_{CC}-30%	—	—	Vdc
Output Low Voltage					
(V_{CC} = min, I_{Load} = 1.6 mAdc)	V_{OL}	—	—	+0.4	Vdc
Output High Current (Sourcing)					
(V_{OH} = 2.4 Vdc)	I_{OH}	-100	—	—	μAdc
Output Low Current (Sinking)					
(V_{OL} = 0.4 Vdc)	I_{OL}	1.6	—	—	mAdc
Input Capacitance					
(V_{in} - 0, T_A = 25°C, f = 1.0 MHz)					
PA, PB, PC, PD, CNTR	C_{in}	—	—	10	pF
XTLI, XTLO		—	—	50	pF
Output Capacitance					
(V_{in} - 0, T_A = 25°C, f = 1.0 MHz)	C_{out}	—	—	10	pF
I/O Port Resistance	R_L	3.0	6.0	11.5	KΩ
PA0-PA7, PB0-PB7, PC0-PC7, PD0-PD7, CNTR					

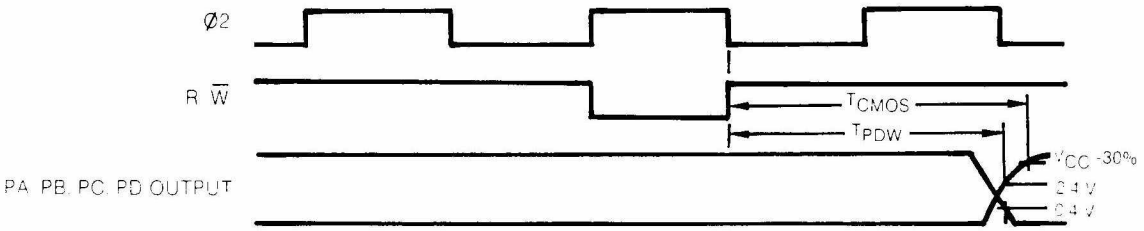
NOTE: Negative sign indicates outward current flow, positive indicates inward flow.

AC CHARACTERISTICS (V_{CC} = 5 V + 5%, T_A = 0° to 70° C)

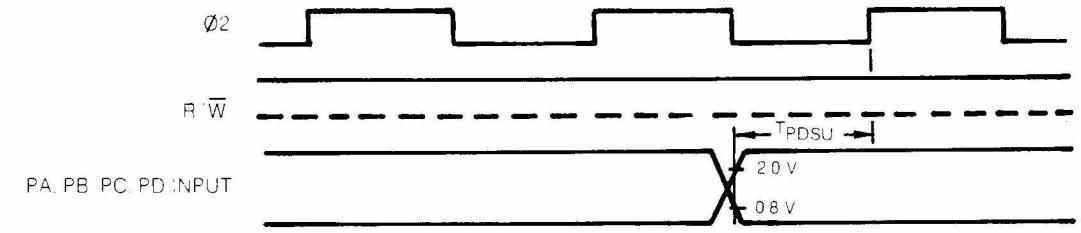
Parameter	Symbol	1 MHz		2 MHz		3 MHz		Unit
		Min	Max	Min	Max	Min	Max	
XTLI Input Clock Cycle Time	T_{cyc}	0.500	5.0	0.250	5.0	0.165	5.0	μsec
Internal Write to Peripheral Data Valid (TTL)	T_{PDW}	1.0	—	0.5	—	0.33	—	μsec
Internal Write to Peripheral Data Valid (CMOS)	T_{CMOS}	2.0	—	1.0	—	0.66	—	μsec
Peripheral Data Setup Time	T_{PDSU}	400	—	200	—	130	—	nsec
Count and Edge Detect Pulse Width	T_{PW}	1.0	—	0.5	—	0.33	—	μsec

TIMING CHARACTERISTICS

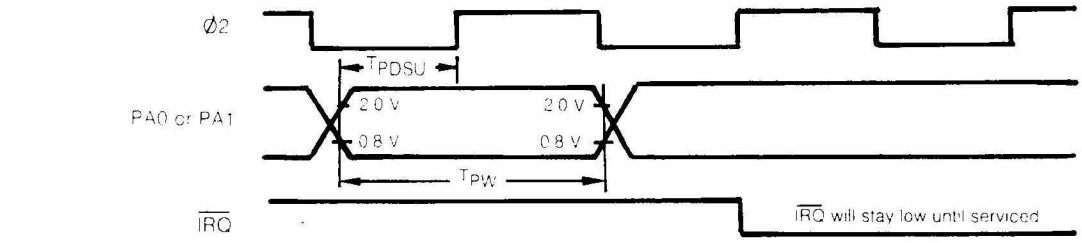
I/O PORT OUTPUT TIMING



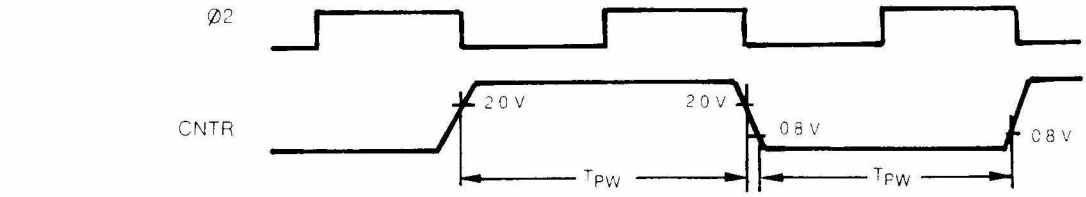
I/O PORT INPUT TIMING



PA0 AND PA1 EDGE DETECT TIMING



EVENT COUNTER TIMING



ORDERING INFORMATION

The following information must be provided when ordering:

Internal Clock Frequency:

External Frequency Reference: ____Crystal or Clock ____RC Network

Pull-Up Options:

I/O Port A	____ Insert	____ Delete
I/O Port B	____ Insert	____ Delete
I/O Port C	____ Insert	____ Delete
I/O Port D	____ Insert	____ Delete
CNTR	____ Insert	____ Delete

Font Verification Media: ____ Paper Tape ____ Card Deck

____ Eprom

____ Other _____
Specify