NEC

MOS INTEGRATED CIRCUIT

μPD16431A

1/2, 1/3, 1/4-DUTY LCD CONTROLLER/DRIVER

The μPD16431A is an LCD controller/driver that enables display of segment type LCDs of 1/2, 1/3, or 1/4 duty cycle. This controller/driver has 56 segment output lines of which eight can also be used as LED output lines. Because the LCD driver contained in the μPD16431A has separate logic and power supply, up to 6.5 V of LCD drive voltage can be set. In addition, key source output lines for key scanning and key input data lines are also provided, so that the μPD16431A is ideal for applications in the front panel of an automobile stereo system.

FEATURES

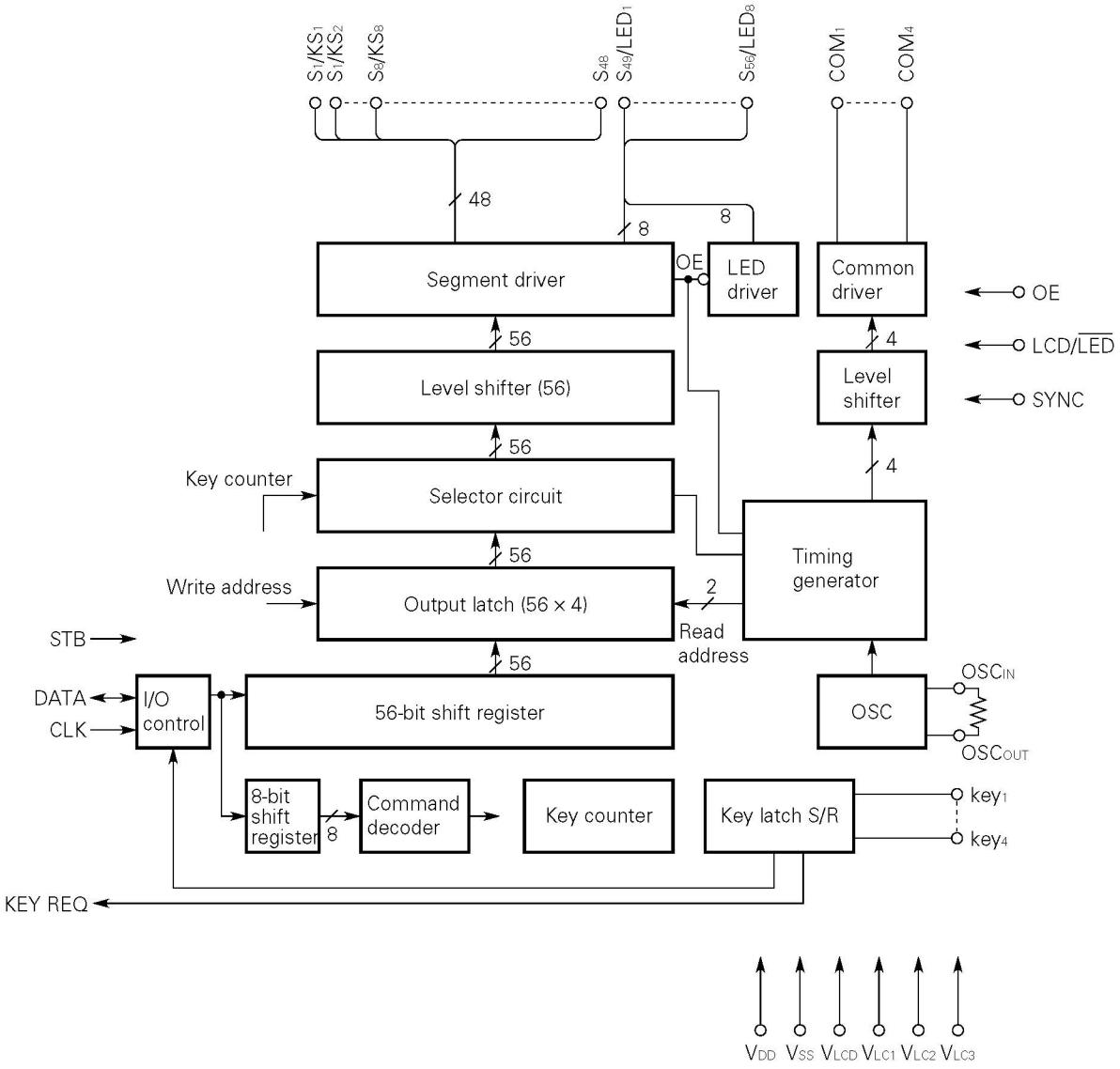
- Various display modes
  - 1/2 duty: 112 segment outputs or 96 segment outputs + 8 LED outputs
  - 1/3 duty: 168 segment outputs or 144 segment outputs + 8 LED outputs
  - 1/4 duty: 224 segment outputs or 192 segment outputs + 8 LED outputs
- Key scan circuit (key source outputs are shared with LCD driver outputs)
- Independent LCD driver power supply V_{LCD} (can be set to V_{DD} to 6.5 V)
- Serial data input/output (SCK, STB, DATA)
- On-chip oscillator incorporated
- Power-ON reset circuit

ORDERING INFORMATION

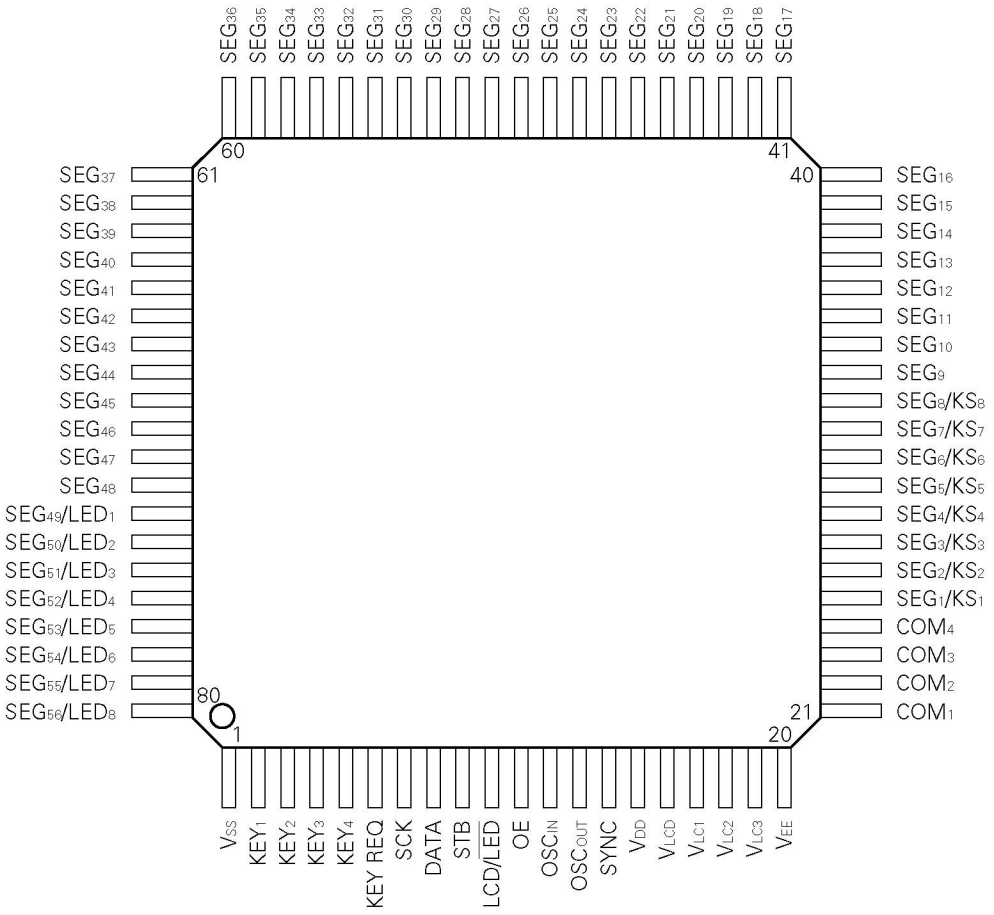
Part Number	Package
μPD16431AGC-7ET	80-pin plastic QFP (0.65 pitch, 14 × 14)

Document No. IC-3414
(O.D. No. IC-8885)
Date Published January 1995 P
Printed in Japan

BLOCK DIAGRAM



PIN CONFIGURATION



Note Though V_{SS} and V_{EE} are internally connected, be sure to connect all the power supply pins (V_{DD}, V_{SS}, V_{LCD}, and V_{EE}).

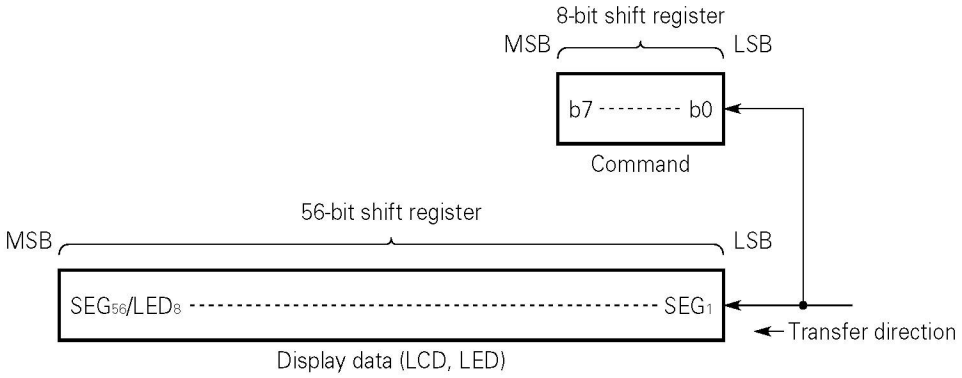
PIN FUNCTIONS

Symbol	Name	No.	Description
SEG_1/KS_1 to SEG_8/KS_8	Segment output/key source output	25 to 32	These pins serve as LCD segment output pins and key source output pins for key scanning.
SEG_9 to SEG_{48}	Segment output	33 to 72	LCD segment output pins
SEG_{49}/LED_1 to SEG_{56}/LED_8	Segment output/LED output pins	73 to 80	These pins can be used as LCD segment output or LED output pins depending on the setting of the LCD/$\overline{LED}$ pin.
COM_1 to COM_4	Common output	21 to 24	LCD common output pins
SCK	Shift clock input	7	Data shift clock. Data is read at the rising edge, and is output at the falling edge of this clock.
DATA	Data input/output	8	This pin inputs a command or display data, or outputs key data. A command or data is input at the rising edge of the shift clock, starting from the most significant bit. Key data is output at the falling edge of the shift clock, starting from the most significant bit. This pin serves as an open-drain pin in the output mode.
STB	Strobe input	9	Data can be input when this signal goes low. When it goes high, command processing is performed.
LCD/$\overline{LED}$	LCD/LED select	10	When this signal goes high, the SEG_n/LED_m pins function as LCD segment output pins; when it goes low, they function as LED driver output pins. The LED driver has a drive capability of 15 mA and is N-ch open drain.
OE Note	Output enable input	11	When this signal goes low, all the segment output and LED output pins are off ($SEG_n = COM_n = V_{LCD}$). Internal data are saved.
OSC_{IN}	Oscillation input	12	Connect a resistor for oscillation circuit across these pins.
OSC_{OUT}	Oscillation output	13	
SYNC	Synchronizing signal	14	A synchronizing signal input pin. When two or more μPD16431A's are used, each device is wired-ORed. This pin must be pulled up when this chip is used alone.
KEY_1 to KEY_4	Key data input	2 to 5	Key data input pins for key scanning
KEY REQ	Key request output	6	This signal goes high when a key is pressed (key data = H). Read the key data only while this pin is high.
V_{DD}	Logic power supply	15	Power supply pin for internal logic
V_{SS}	Logic GND	1	GND pin for internal logic and LED output
V_{LCD}	LCD drive power supply	16	Power supply pin for LCD drive
V_{EE}	LCD GND	20	GND pin for LCD drive
V_{LC1} to V_{LC3}	Power supply for LCD drive	17 to 19	Power supply for driving dot matrix LCD

Note At OE = L, the key data cannot be written correctly, even when the display ON/OFF of the status command is set to the "normal operation" (10). Also, in this state, unnecessary waveforms are generated from between SEG_1/KS_1 to SEG_8/KS_8 during the key scanning period. (The display is OFF.)

CONFIGURATION OF SHIFT REGISTER

Two shift registers, an 8-bit command register and a 56-bit display register, are provided. The first 8 bits of input data are recognized as a command and are sent to the command register, and the 9th bit and those that follow are recognized as display data and are sent to the display register.



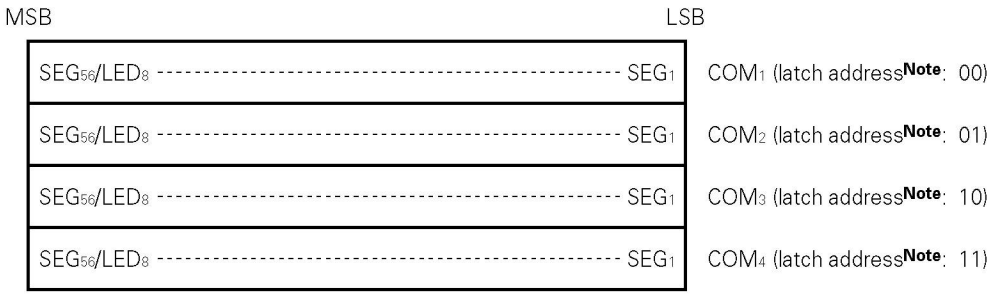
The meaning of the display data is as follows:

LCD: 0 → off, 1 → on

LED: 0 → on, 1 → off

Be sure to transfer 56 bits of display data.

CONFIGURATION OF OUTPUT LATCH



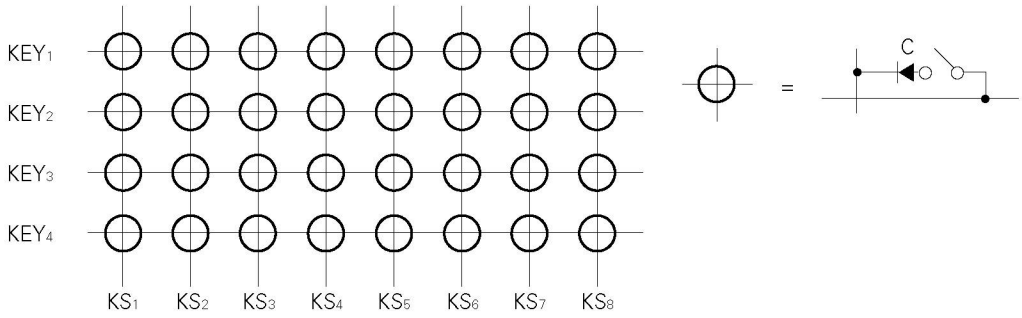
Note Bits b3 and b4 of status command (Refer to page 8.)

KEY MATRIX CONFIGURATION

An example of key matrix configurations is shown below.

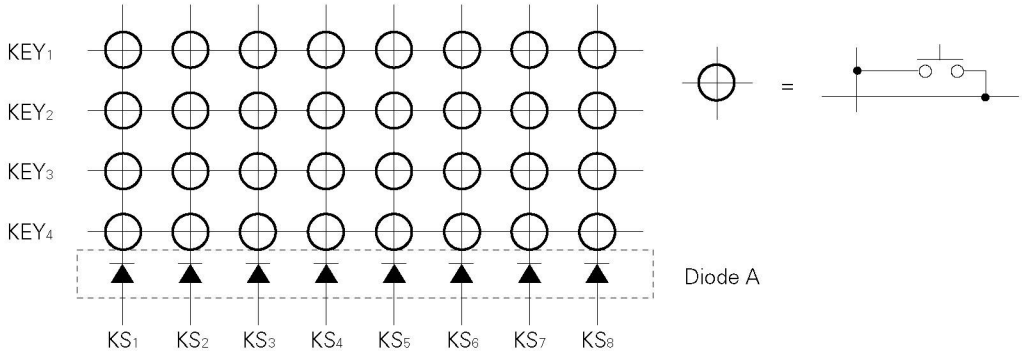
1) **When pressing three or more times is assumed:**

A configuration example is shown below. In this configuration, 0 to 32 ON switches can be recognized.



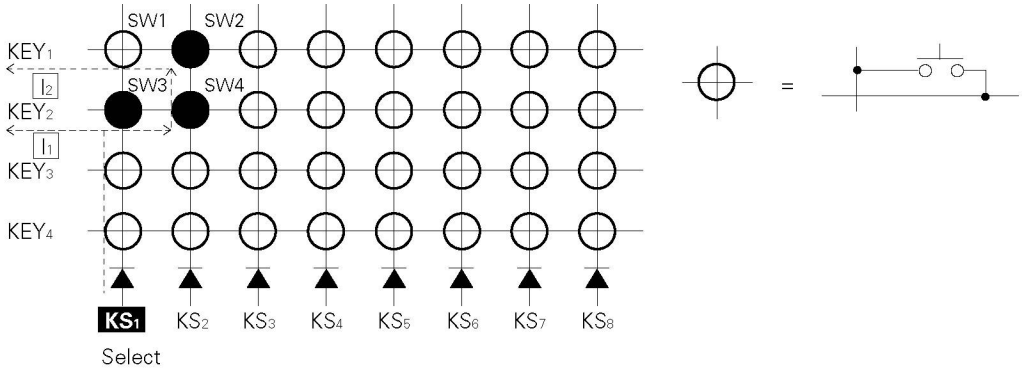
2) **When pressing twice or more times is assumed:**

A configuration example is shown below. In this configuration, 0 to 2 ON switches can be recognized.



In this configuration, pressing three or more times may cause OFF switches to be determined to be ON.

For example, if SW2 to SW4 are ON and KS1 has been selected (high level) as shown below, SW3 in which current I1 is running is supposed to be detected to be ON. However, since SW2 and SW4 are ON, current I2 runs thus resulting in SW1 to be recognized as being ON.



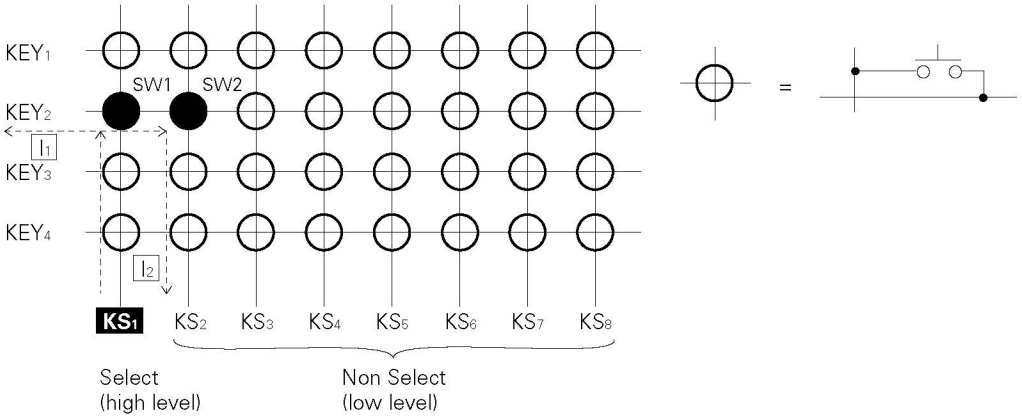
If diode A is not available, not only the key data may not be read normally but the LCD display may be affected or ICs may be damaged or deteriorated.

For example, if SW1 and SW2 are ON and KS_1 has been selected (high level) as shown below, this will cause not only current I_1 which is supposed to run but also short-circuited current I_2 of KS_1 to KS_2 to run. It is possible that this will then cause the following three problems:

(1)Since the level to KEY_2 is not correctly sent, the key data cannot be latched correctly.

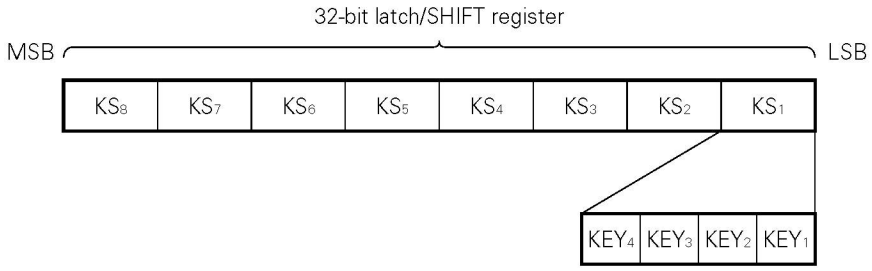
(2)If KS_2 is used as SEG_2 as well, the LCD display may be distorted (such as causing unintended segments to light up).

(3)Since the short-circuited current (current I_2) of KS_2 (high level) to KS_2 (low level) runs, ICS may be damaged or deteriorated



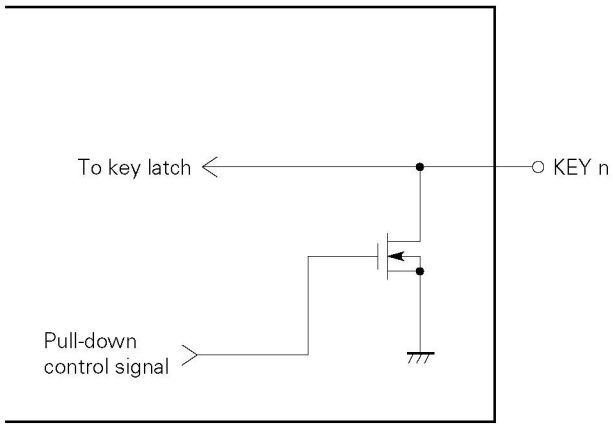
CONFIGURATION OF KEY DATA LATCH

The key data is latched as illustrated below and is read by a read command, starting from the most significant bit. Key data is read once a frame and latched when coinciding with the immediadtely preceding data. In other words, it requires at least 2 frames from the time the key is pressed till data is confirmed to be the key data (the key request becoming H).



The key data is 0 when off and 1 when on.

KEY INPUT EQUIVALENT CIRCUIT



- The pull-down control signal goes high only during key source output and turns on the pull-down transistor.
- The on-resistance of the pull-down transistor is several kΩ.

COMMAND

A command sets a display mode and a status.

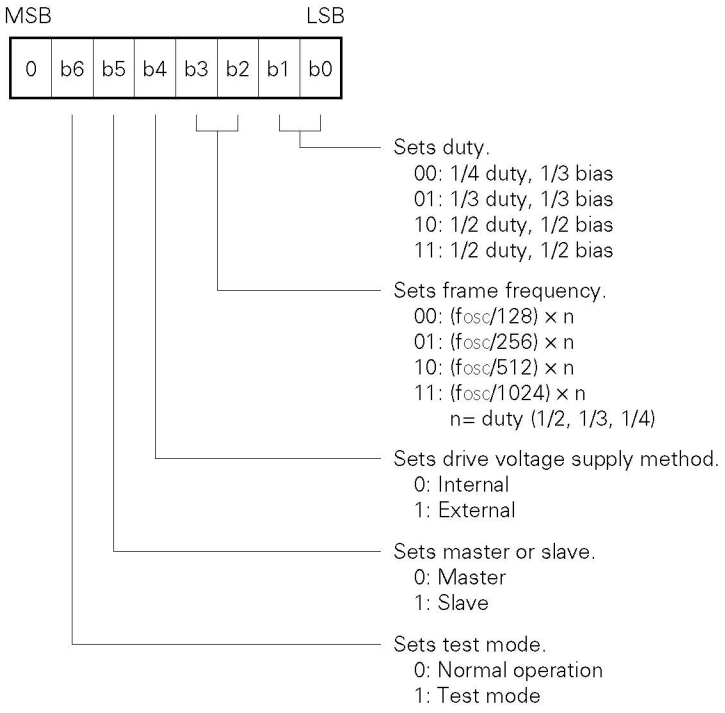
The first 1 byte input after the STB pin has fallen is regarded as a command.

If the STB pin is made low while a command/data is transferred, serial communication is initialized, and the command/data being transferred is made invalid (the command/data that has been already transferred remains valid, however).

(1) Display setting command

This command initializes the μPD16431A and sets a duty cycle, frame frequency, drive voltage supply method, test mode, and whether the μPD16431A operates as the master or a slave.

When this command is executed, display is forcibly turned off and key scanning is stopped. To resume the display, the normal operation of the "status command" must be executed. Note, however, that nothing is executed if the same mode is selected.

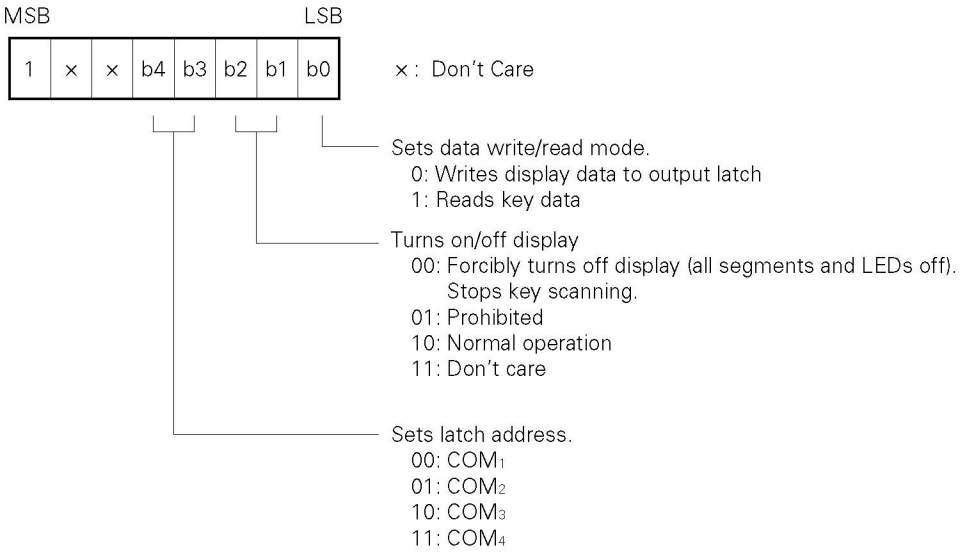


Values when power is applied

	0	0	0	0	0	0	0

(2) Status command

This command sets a data write/read mode, turns on/off display, and sets a latch address.



Values when power is applied

	×	×	0	0	0	0	0

OUTPUT SELECT VOLTAGE

1. COM

	+	−	Bias
When selected	V_{LCD} V_{LCD}	GND GND	1/2 bias
When not selected	1/2 V_{LCD} V_{LC2}	1/2 V_{LCD} V_{LC2}	
When key scanned	1/2 V_{LCD} V_{LC2}	1/2 V_{LCD} V_{LC2}	
When selected	V_{LCD} V_{LCD}	GND GND	1/3 bias
When not selected	1/3 V_{LCD} V_{LC3}	2/3 V_{LCD} V_{LC1}	
When key scanned	1/2 V_{LCD} V_{LC2}	1/2 V_{LCD} V_{LC2}	

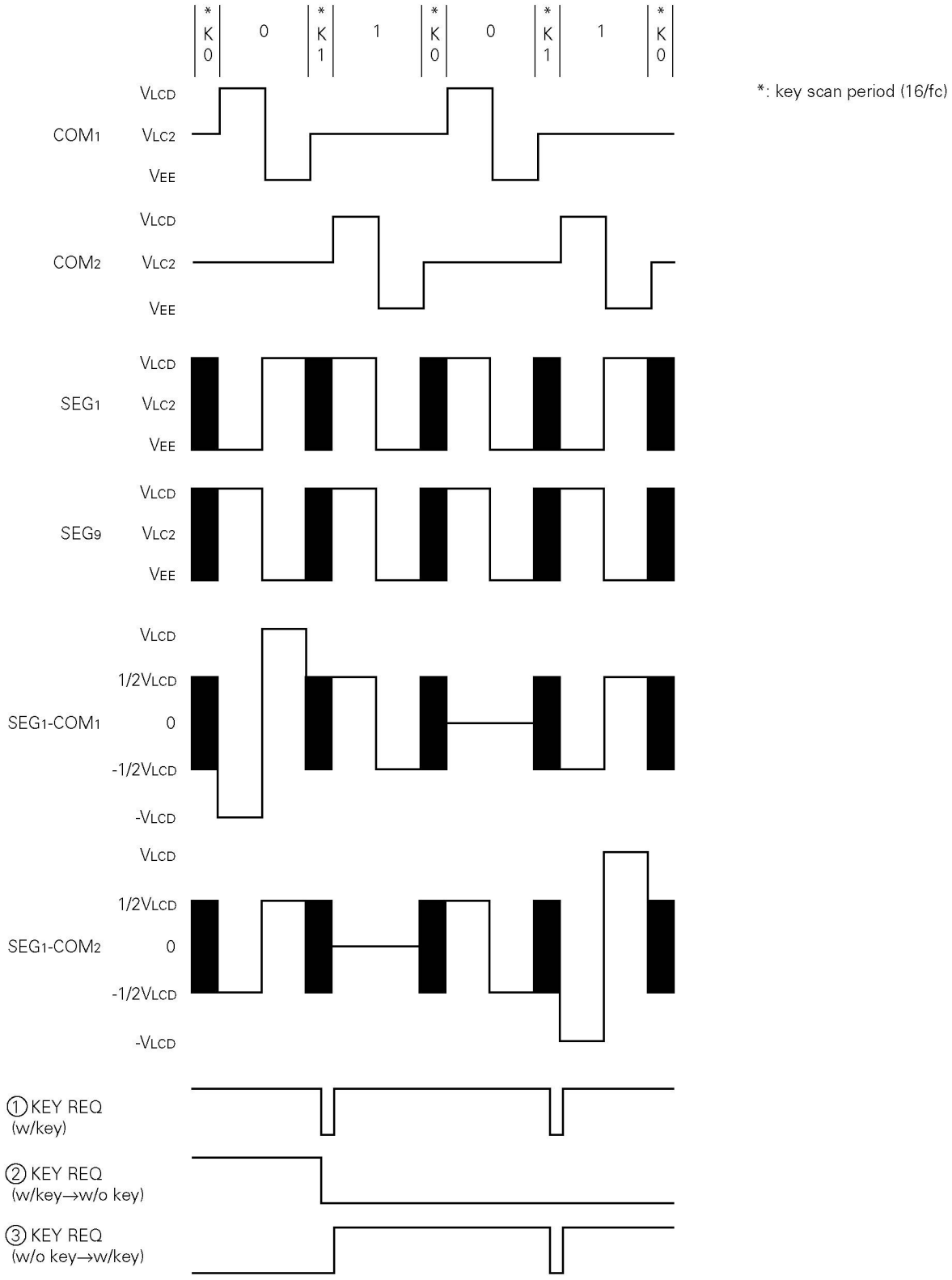
Top : with internal power supply
Bottom: with external power supply

2. SEG

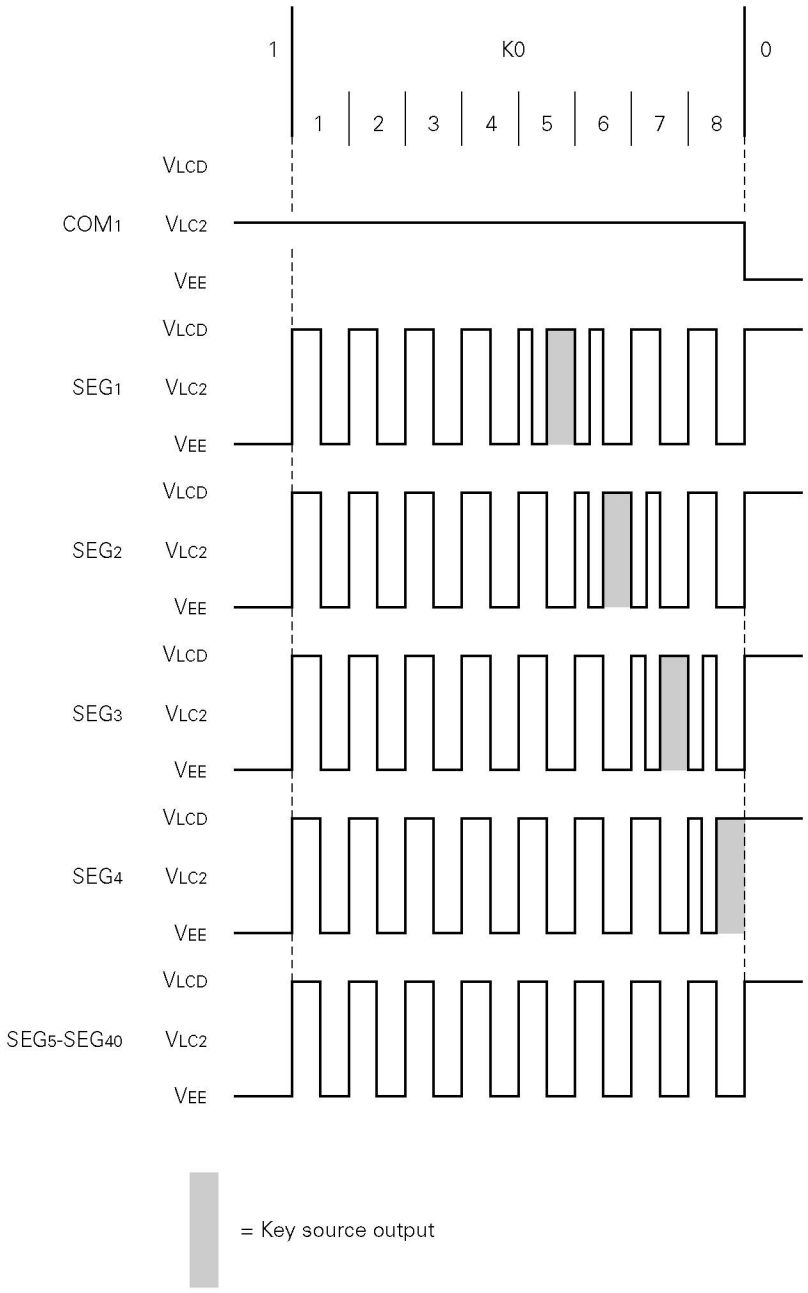
	+	−	Bias
When selected	GND GND	V_{LCD} V_{LCD}	1/2 bias
When not selected	V_{LCD} V_{LCD}	GND GND	
When key scanned	GND GND	V_{LCD} V_{LCD}	
When key not scanned	V_{LCD} V_{LCD}	GND GND	
When selected	GND GND	V_{LCD} V_{LCD}	1/3 bias
When not selected	2/3 V_{LCD} V_{LC1}	1/3 V_{LCD} V_{LC3}	
When key scanned	GND GND	V_{LCD} V_{LCD}	
When key not scanned	V_{LCD} V_{LCD}	GND GND	

OUTPUT WAVEFORM

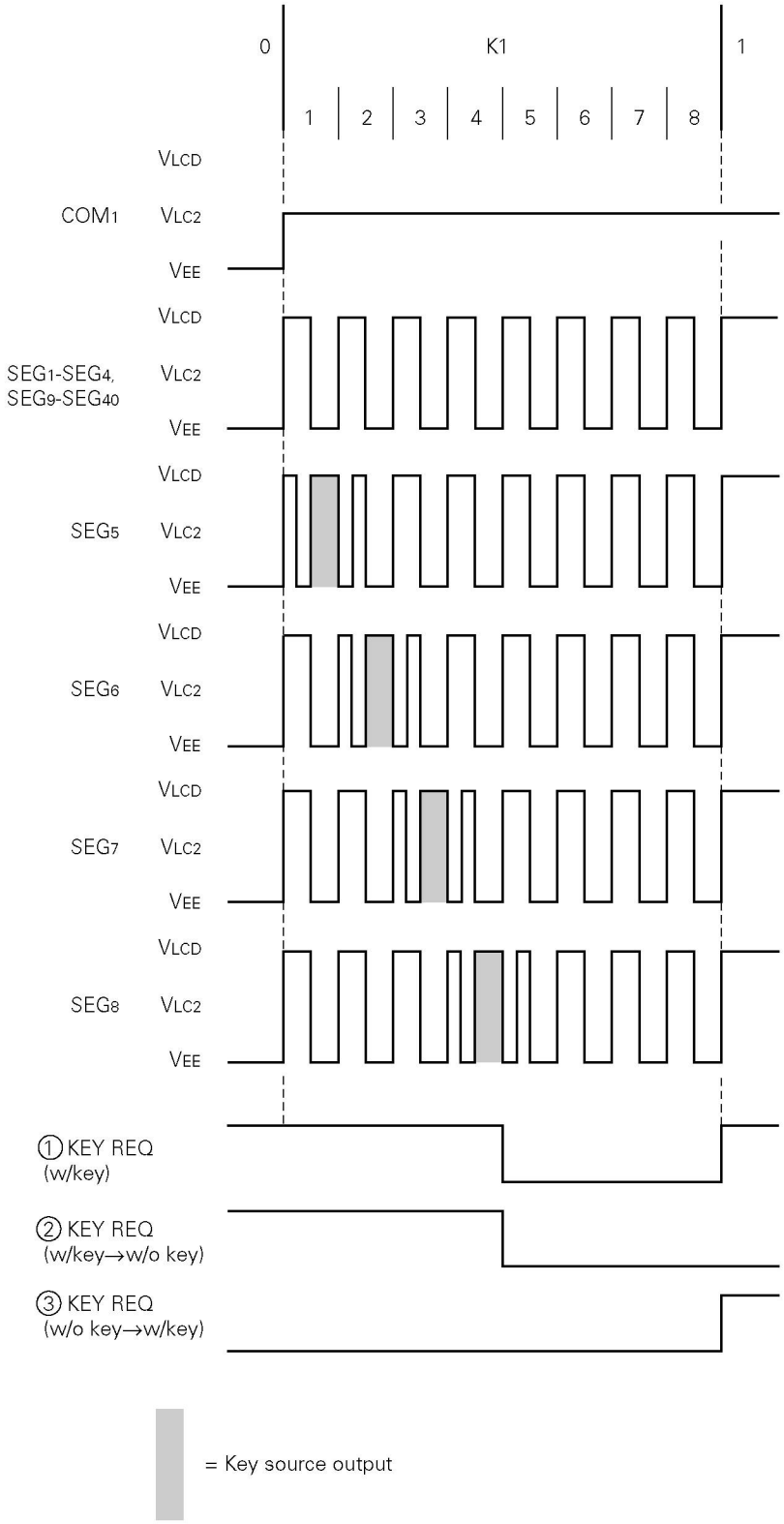
(1) 1/2 duty (1/2 dias)



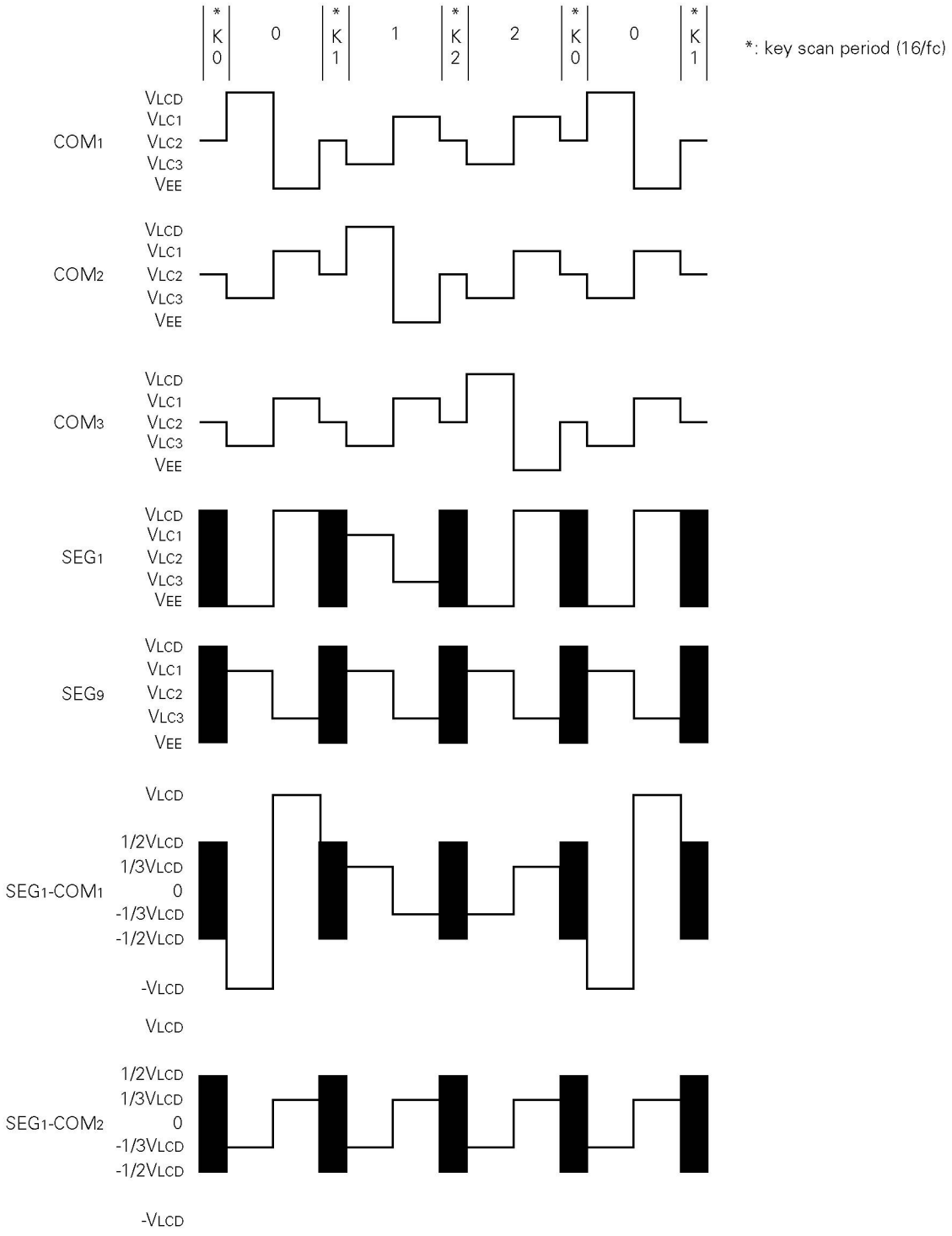
KEY SCAN PERIOD (K0) EXPANSION



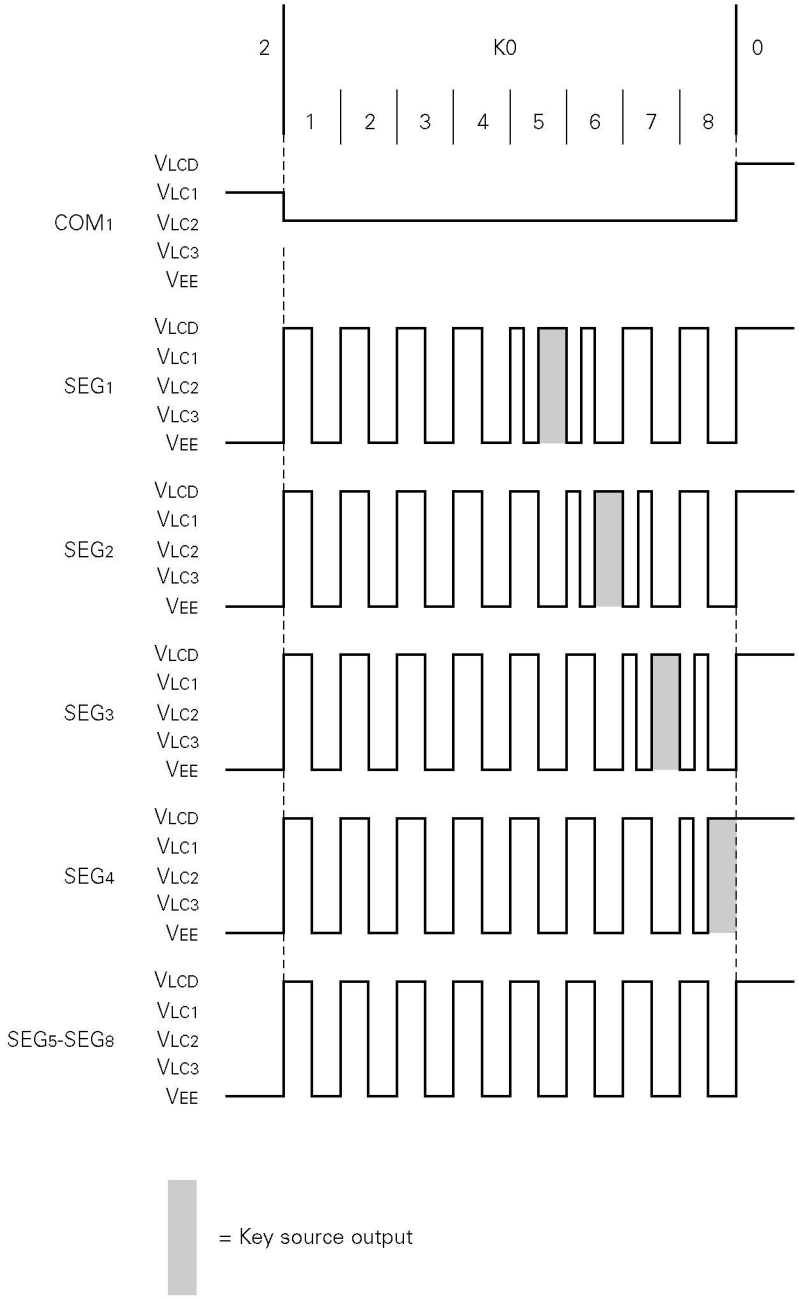
KEY SCAN PERIOD (K1) EXPANSION



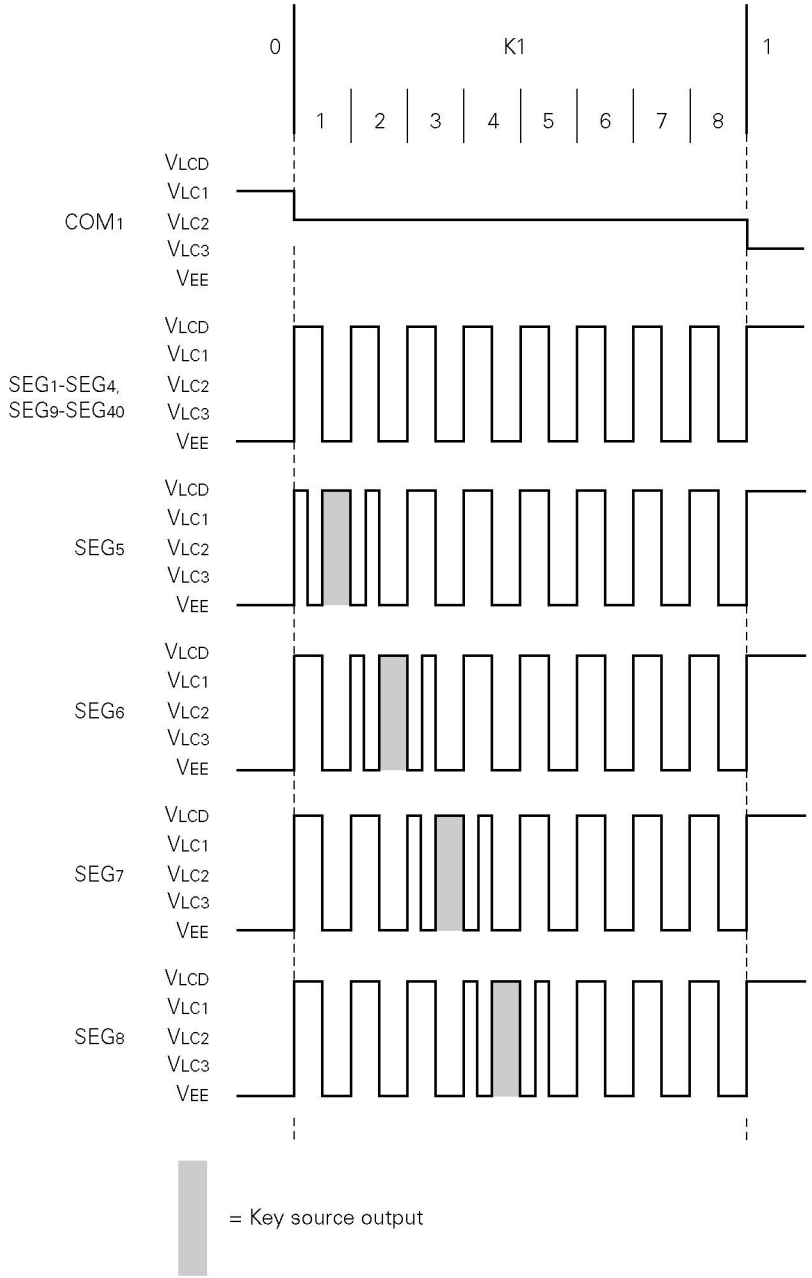
(2) 1/3 duty (1/3 bias)



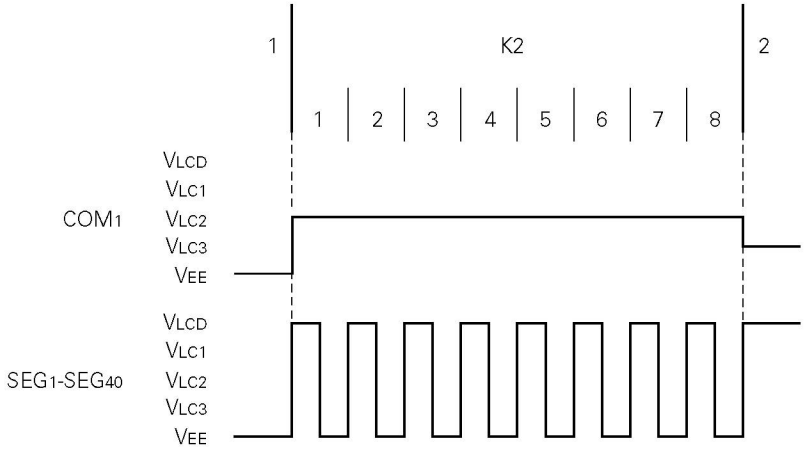
KEY SCAN PERIOD (K0) EXPANSION



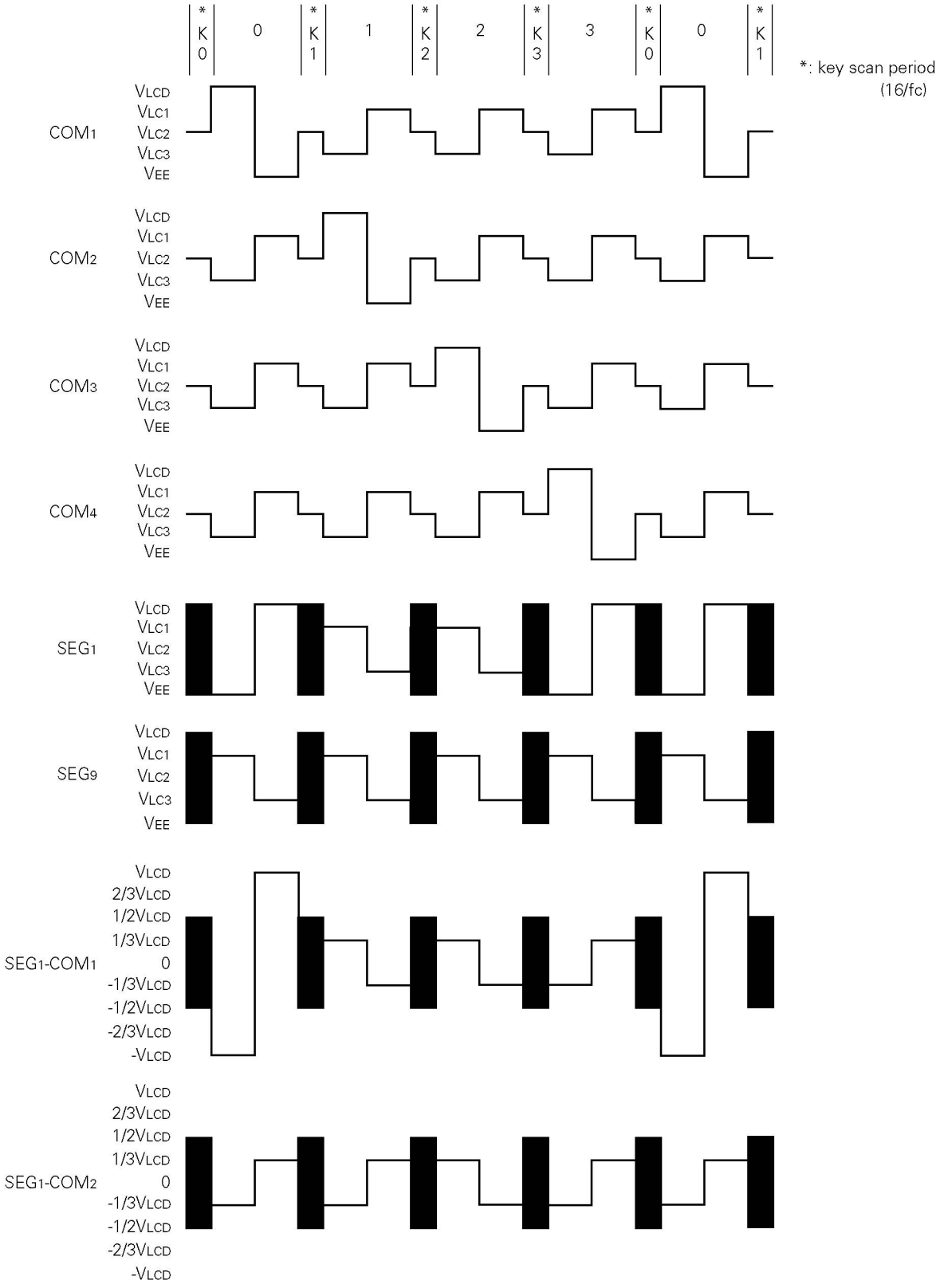
KEY SCAN PERIOD (K1) EXPANSION



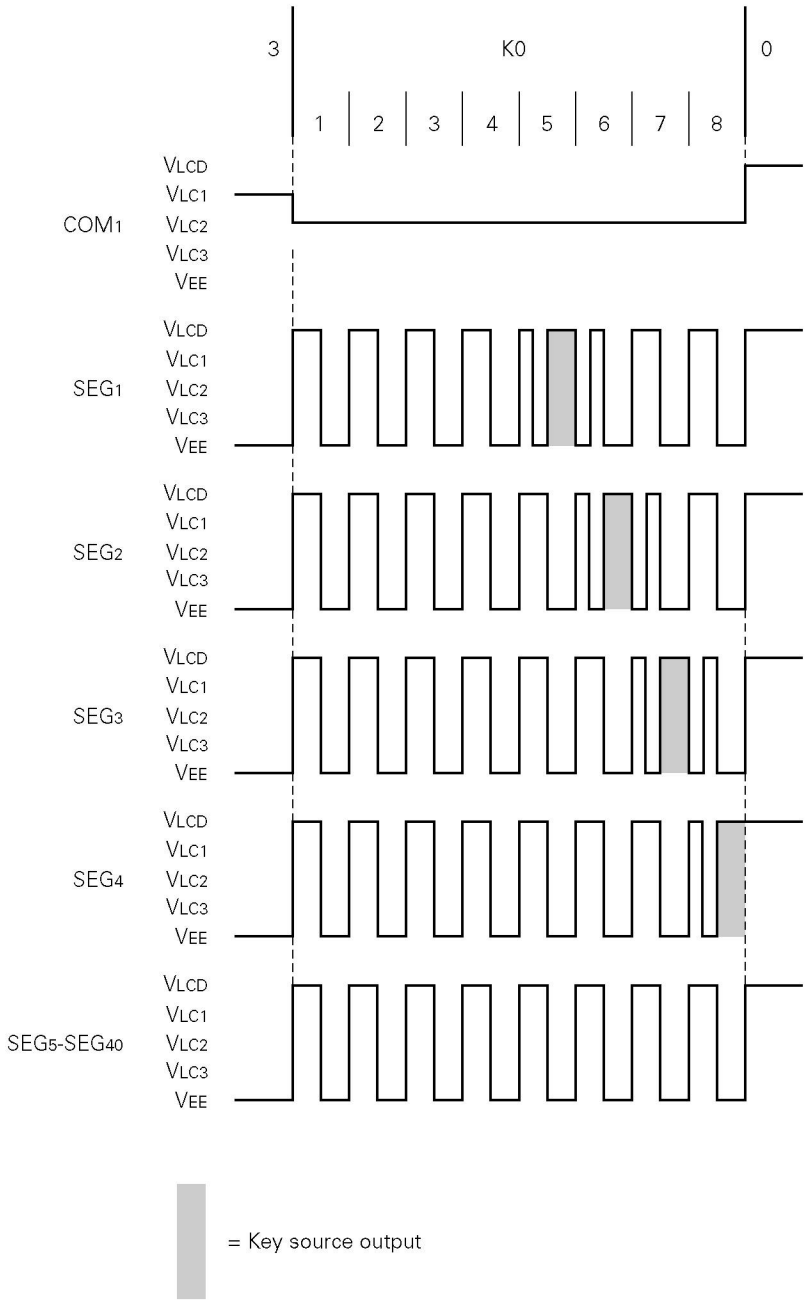
KEY SCAN PERIOD (K2) EXPANSION



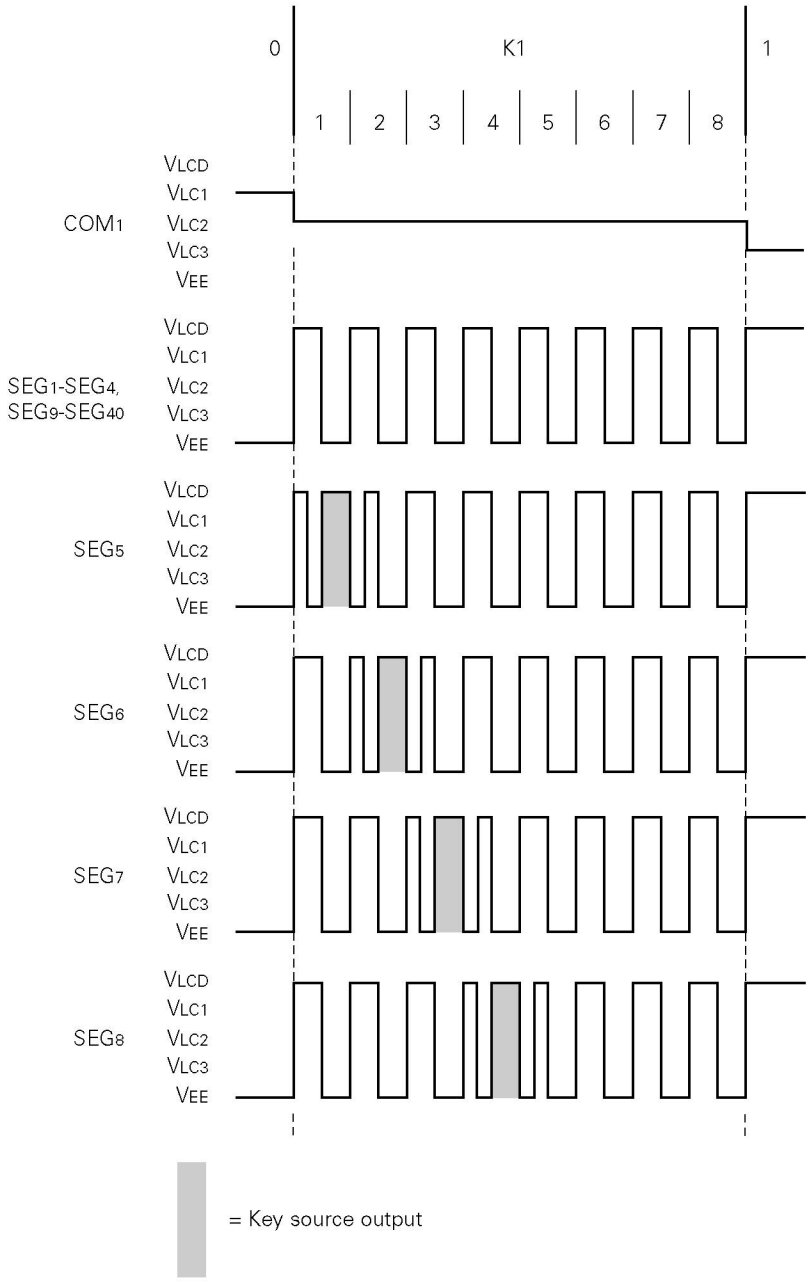
(3) 1/4 duty (1/3 bias)



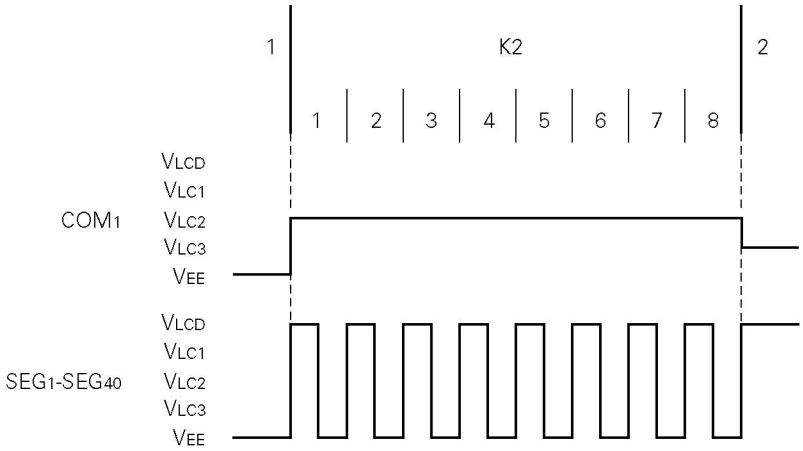
KEY SCAN PERIOD (K0) EXPANSION



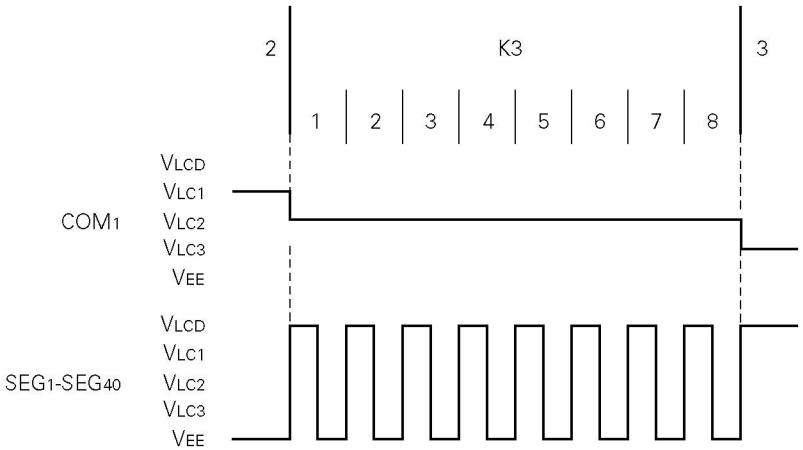
KEY SCAN PERIOD (K1) EXPANSION



KEY SCAN PERIOD (K2) EXPANSION

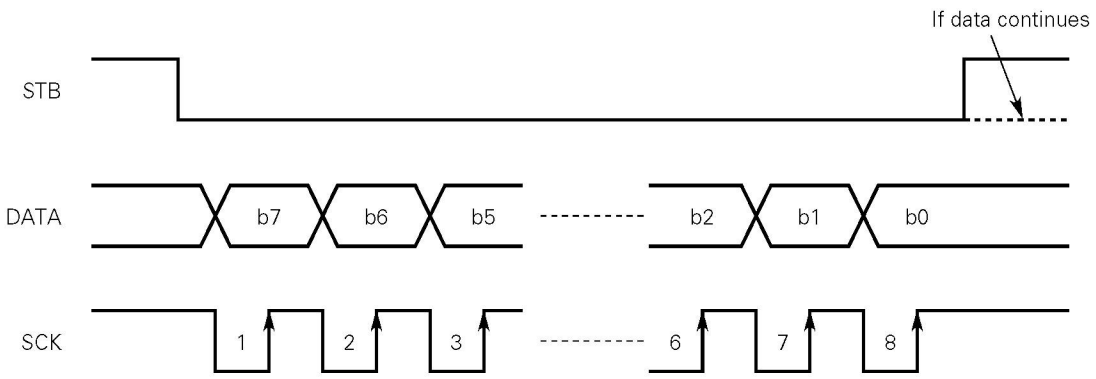


KEY SCAN PERIOD (K3) EXPANSION

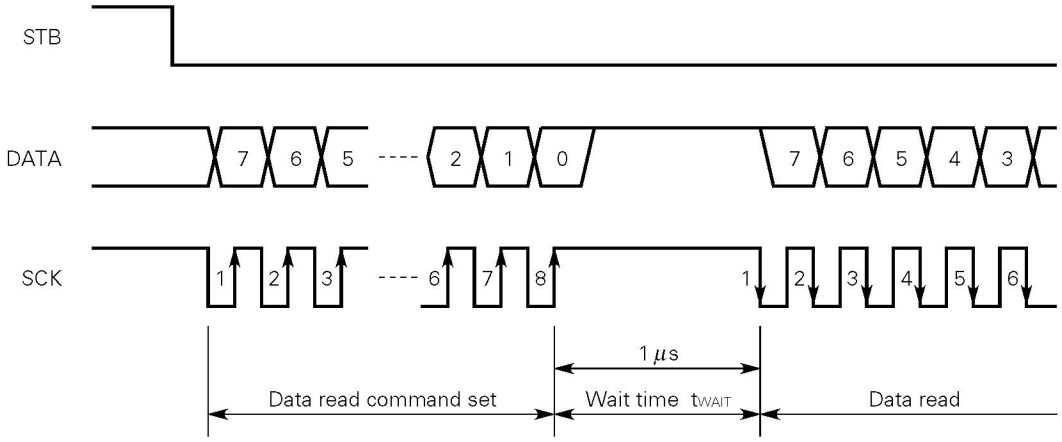


SERIAL COMMUNICATION FORMAT

(1) Receive (command/data write)



(2) Transmit (command/data read)



Note Because the DATA pin is an N-ch open-drain output pin, be sure to connect an external pull-up resistor to this pin (1 kΩ to 10 kΩ).

APPLICATION

1. Example of initial setting + display data write

Parameter	STB	Command/data b7	b6	b5	b4	b3	b2	b1	b0	Remarks
Start	H									
Set display command	L	0	0	0	0	0	0	0	0	1/4 duty, frame frequency = fosc/128 × 1/4, internal drive voltage, master
	H									
Status command	L	1	0	0	0	0	0	0	0	Display data write, display off, latch address: COM_1
Display data 1	L	×	×	×	×	×	×	×	×	COM_1 data (7 bytes)
⋮	⋮									
Display data 7	L	×	×	×	×	×	×	×	×	
	H									
Status command	L	1	0	0	0	1	0	0	0	Display data write, display off, latch address: COM_2
Display data 1	L	×	×	×	×	×	×	×	×	COM_2 data (7 bytes)
⋮	⋮									
Display data 7	L	×	×	×	×	×	×	×	×	
	H									
Status command	L	1	0	0	1	0	0	0	0	Display data write, display off, latch address: COM_3
Display data 1	L	×	×	×	×	×	×	×	×	COM_3 data (7 bytes)
⋮	⋮									
Display data 7	L	×	×	×	×	×	×	×	×	
	H									
Status command	L	1	0	0	1	1	0	0	0	Display data write, display off, latch address: COM_4
Display data 1	L	×	×	×	×	×	×	×	×	COM_4 data (7 bytes)
⋮	⋮									
Display data 7	L	×	×	×	×	×	×	×	×	
	H									
Status command	L	1	0	0	0	0	1	0	0	Display data write, display on
End	H									

2. Example of display data write (rewrite, 1/4)

Parameter	STB	Command/data								Remarks
		b7	b6	b5	b4	b3	b2	b1	b0	
Start	H									
Status command	L	1	0	0	0	0	1	0	0	Display data write, display on, latch address: COM_1
Display data 1	L	×	×	×	×	×	×	×	×	COM_1 data (7 bytes)
⋮	⋮									
Display data 7	L	×	×	×	×	×	×	×	×	
	H									
Status command	L	1	0	0	0	1	1	0	0	Display data write, display on, latch address: COM_2
Display data 1	L	×	×	×	×	×	×	×	×	COM_2 data (7 bytes)
⋮	⋮									
Display data 7	L	×	×	×	×	×	×	×	×	
	H									
Status command	L	1	0	0	1	0	1	0	0	Display data write, display on, latch address: COM_3
Display data 1	L	×	×	×	×	×	×	×	×	COM_3 data (7 bytes)
⋮	⋮									
Display data 7	L	×	×	×	×	×	×	×	×	
	H									
Status command	L	1	0	0	1	1	1	0	0	Display data write, display on, latch address: COM_4
Display data 1	L	×	×	×	×	×	×	×	×	COM_4 data (7 bytes)
⋮	⋮									
Display data 7	L	×	×	×	×	×	×	×	×	
End	H									

3. Example of key data read

Parameter	STB	Command/data b7	b6	b5	b4	b3	b2	b1	b0	Remarks
KEY REQ check										KEY REQ = H: Key data exists. → Start reading. KEY REQ = L: Key data does not exist (reading is inhibited). → Check KEY REQ again.
Start	H									
Status command	L	1	0	0	0	0	1	0	1	Data read, display on
Wait time	L									1 μs
Key data 1	L	×	×	×	×	×	×	×	×	4 bytes
⋮	⋮									
Key data 4	L	×	×	×	×	×	×	×	×	
End	H									

ABSOLUTE MAXIMUM RATINGS (T_a = 25 °C, V_{SS} = 0 V)

Parameter	Symbol	Ratings	Unit
Logic supply voltage	V_{DD}	–0.3 to +7.0	V
Logic input voltage	V_{IN}	–0.3 to V_{DD} + 0.3	V
Logic output voltage (DATA)	V_{OUT}	–0.3 to +7.0	V
LCD drive supply voltage	V_{LCD}	–0.3 to +7.0	V
LCD drive supply input voltage	V_{LC1} to V_{LC3}	–0.3 to V_{LCD} + 0.3	V
Driver output voltage (segment, common, LED)	V_{OUT2}	–0.3 to V_{LCD} + 0.3	V
LED output current	I_O	+20	mA
Operating ambient temperature	T_{opt}	–40 to +85	°C
Storage temperature	T_{stg}	–55 to +150	°C
Permissible package power dissipation	P_T	1 000	mW

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Logic supply voltage	V_{DD}	2.7	5.0	5.5	V
LCD drive supply voltage	V_{LCD}	V_{DD}	5.0	6.5	V
Logic input voltage	V_{IN}	0		V_{DD}	V
Driver output voltage	V_{LC1} to V_{LC3}	0		V_{LCD}	V

ELECTRICAL SPECIFICATIONS (Unless otherwise specified, T_a = –40 to +85 °C, V_{DD} = V_{LCD} = 5 V ±10%)

Parameter	Symbol		MIN.	TYP.	MAX.	Unit
Input voltage, high	V_{IH}		0.7 V_{DD}		V_{DD}	V
Input voltage, low	V_{IL}		0		0.3 V_{DD}	V
Input current, high	I_{IH}	CLK, STB, LCD/$\overline{\text{LED}}$, OE			1	μA
Input current, low	I_{IL}	CLK, STB, LCD/$\overline{\text{LED}}$, OE			–1	μA
Output voltage, low	V_{OL1}	LED_1 to LED_8. I_{OL1} = 15 mA			1.0	V
Output voltage, high	V_{OH2}	OSC_{OUT}, I_{OH2} = –1 mA	0.9 V_{DD}			V
Output voltage, low	V_{OL2}	DATA, OSC_{OUT}, SYNC, I_{OL2} = 4 mA			0.1 V_{DD}	V
Leakage current, high	I_{LOH2}	DATA, SYNC, $V_{IN\ OUT}$ = V_{DD}			1	mA
Leakage current, low	I_{LOL2}	DATA, SYNC, $V_{IN\ OUT}$ = V_{SS}			–1	mA
Common output ON resistance	R_{COM}	COM_1 to COM_4, $\lvert I_O \rvert$ = 100 μA			2.4	kΩ
Segment output ON resistance	R_{SEG}	SEG_1 to SEG_{56}, $\lvert I_O \rvert$ = 100 μA			4.0	kΩ
Logic current dissipation	I_{DD}	f_{OSC} = 250 kHz			250	μA
LCD drive current consumption	I_{LCD}	With internal bias and no load			500	μA

Remark The TYP. value is a reference value at T_a = 25 °C.

SWITCHING CHARACTERISTICS

(Unless otherwise specified, T_a = –40 to +85 °C, V_{DD} = V_{LCD} = 5 V ±10%, R_L = 5 kΩ, C_L = 150 pF)

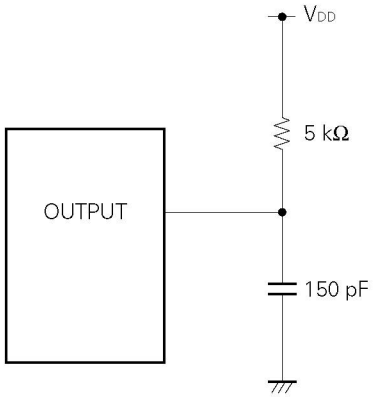
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Oscillation frequency	f_{OSC}	R = 100 kΩ	175	250	325	kHz
Oscillation frequency	f_{OSC}	R = 200 kΩ	105	150	195	kHz
Propagation delay time	t_{PZL}	SCK ↓ → DATA ↓			100	ns
Propagation delay time	t_{PLZ}	SCK ↓ → DATA ↑			300	ns
SYNC delay time	t_{DSYNC}				1.5	μs

TIMING REQUIREMENTS

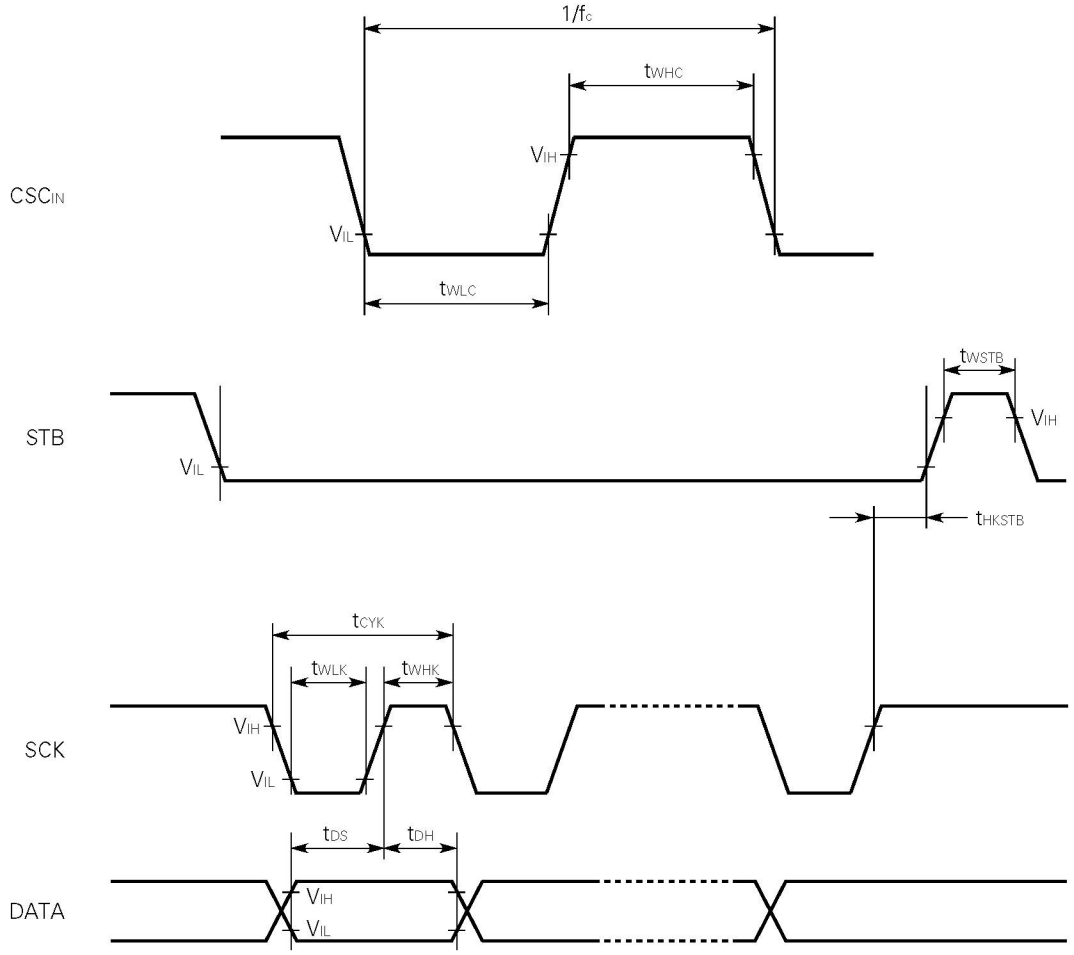
(Unless otherwise specified, T_a = –40 to +85 °C, V_{DD} = V_{LCD} = 5 V ±10%, R_L = 5 kΩ, C_L = 150 pF)

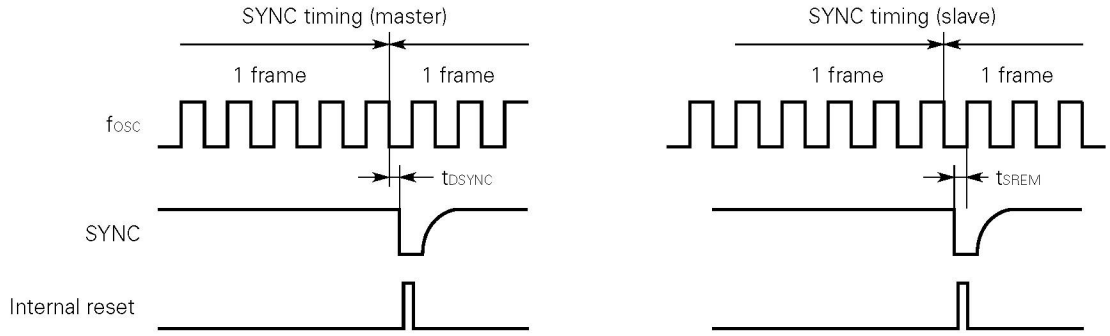
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Clock frequency	f_C	OSC_{IN} external clock	50		325	kHz
High-level clock pulse width	t_{WHC}	OSC_{IN} external clock	1.5		16	μs
Low-level clock pulse width	t_{WLC}	OSC_{IN} external clock	1.5		16	μs
Shift clock cycle	t_{CYK}	SCK	900			ns
High-level shift clock pulse width	t_{WHK}	SCK	400			ns
Low-level shift clock pulse width	t_{WLK}	SCK	400			ns
Shift clock hold time	t_{HSTBK}	STB ↓ → SCK ↓	1.5			μs
Data setup time	t_{DS}	DATA → SCK ↑	100			ns
Data hold time	t_{DH}	SCK ↑ → DATA	200			ns
STB hold time	t_{DKSTB}	SCK ↑ → STB ↑	1			μs
STB pulse width	t_{WSTB}		1			μs
Wait time	t_{WAIT}	CLK ↑ → CLK ↓	1			μs
SYNC removal time	t_{SREM}		250			ns

Output Load

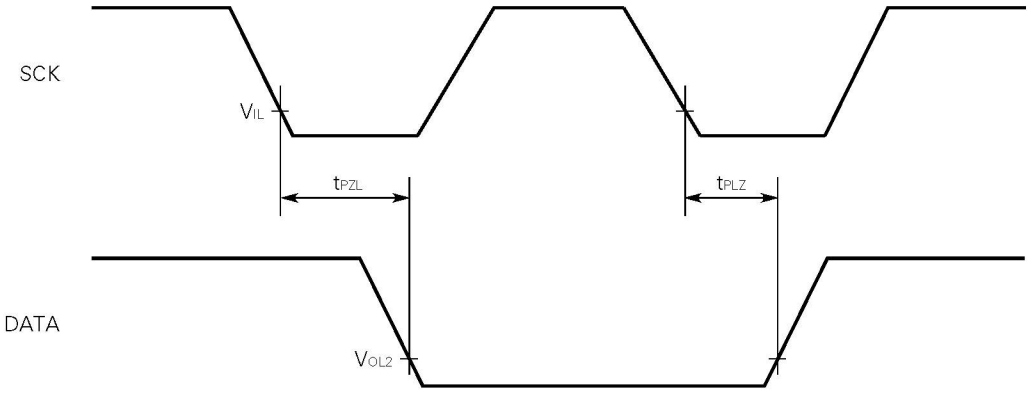


Switching Characteristic Waveform

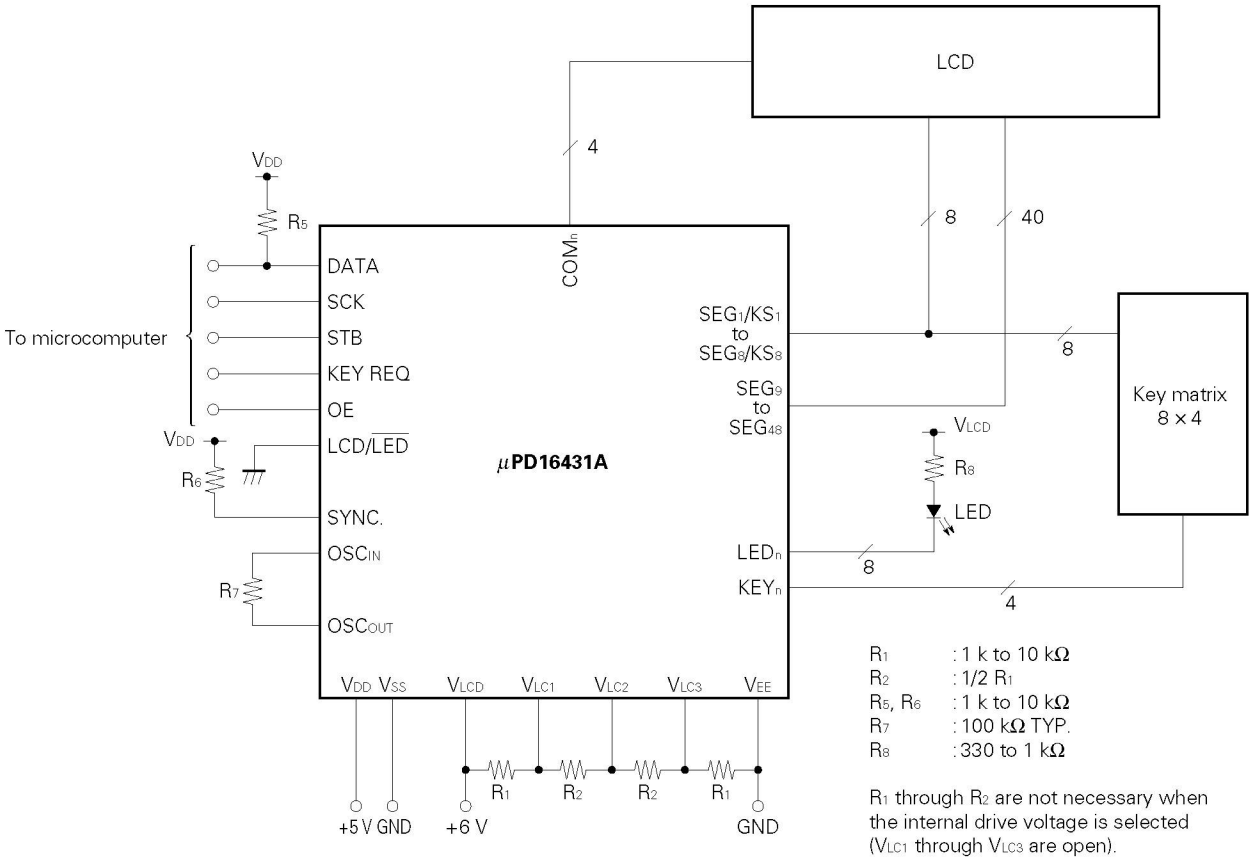




Switching Characteristic Waveform



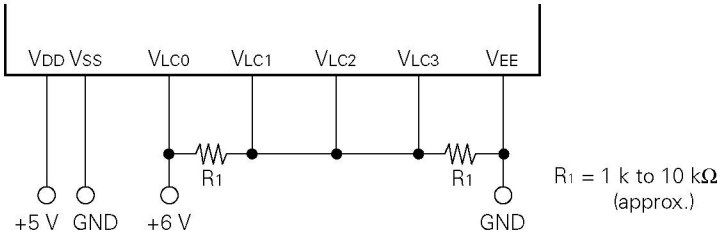
Application Circuit Example (with LED, 1/4 duty, 1/3 bias)



R1 : 1 k to 10 kΩ
R2 : 1/2 R1
R5, R6 : 1 k to 10 kΩ
R7 : 100 kΩ TYP.
R8 : 330 to 1 kΩ

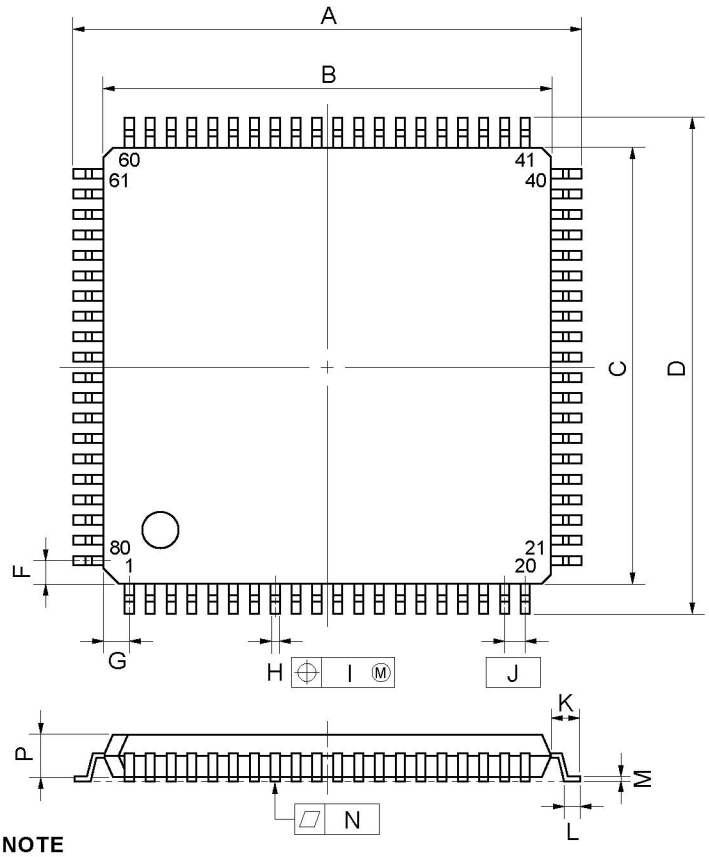
R1 through R2 are not necessary when the internal drive voltage is selected (VLC1 through VLC3 are open).

Note Example of external source circuit (when 1/2 bias)

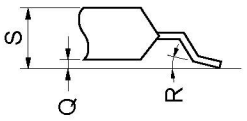


The application circuits and their parameters are for references only and are not intended for use in actual design-in's.

80 PIN PLASTIC LQFP (□14)



detail of lead end



NOTE

Each lead centerline is located within 0.13 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	16.0±0.2	0.630±0.008
B	14.0±0.1	$0.551^{+0.005}_{-0.004}$
C	14.0±0.1	$0.551^{+0.005}_{-0.004}$
D	16.0±0.2	0.630±0.008
F	0.825	0.032
G	0.825	0.032
H	0.30±0.10	$0.012^{+0.004}_{-0.005}$
I	0.13	0.005
J	0.65 (T.P.)	0.026 (T.P.)
K	1.0±0.2	$0.039^{+0.009}_{-0.008}$
L	0.5±0.2	$0.020^{+0.008}_{-0.009}$
M	$0.125^{+0.10}_{-0.05}$	$0.005^{+0.004}_{-0.002}$
N	0.10	0.004
P	1.4±0.1	0.055±0.004
Q	0.125±0.075	0.005±0.003
R	$3^{\circ}{}^{+7^{\circ}}_{-3^{\circ}}$	$3^{\circ}{}^{+7^{\circ}}_{-3^{\circ}}$
S	1.7 MAX.	0.067 MAX.

S80GC-65-7ET-1

REFERENCE

Document Name	Document No.
NEC Semiconductor Device Reliability/Quality Control System	IEI-1212
Quality grade on NEC Semiconductor Devices	IEI-1209

M4 94.11