NEC

MOS INTEGRATED CIRCUIT

μPD16432B

1/8, 1/15 DUTY LCD CONTROLLER/DRIVER

DESCRIPTION

The μPD16432B is a controller/driver with 1/8 and 1/15 duty dot matrix LCD display capability. It has 60 segment outputs, 10 common outputs, and 5 dual segment/common outputs, giving a maximum display capability of 12 columns × 2 lines (at 1/15 duty).

LED drive outputs, key scanning key source outputs, and key data inputs are also provided, making it ideal for use in a car stereo front panel, etc.

FEATURES

- Dot matrix LCD controller/driver
- Pictograph display segment drive capability (max. 64)
- LCD driver unit power supply V_{LCD} independently settable (Max. 10 V)
- On-chip key scan circuit (8 × 4 matrix)
- Alphanumeric character and symbol display capability provided by on-chip ROM (5 × 7 dots)
  240 characters + 16 user-defined characters
- Display contents
  1/8 duty: 13 columns × 1 line, 64 pictograph displays, 4 LEDs
  1/15 duty: 12 columns × 2 lines, 60 pictograph displays, 4 LEDs
- Serial data input/output (SCK, STB, DATA)
- On-chip oscillator
- Reduced power consumption possible using standby mode

ORDERING INFORMATION

Part Number	Package
μPD16432BGC-001-9EU	100-pin plastic QFP (0.5 pitch, 14 × 14), Standard ROM code

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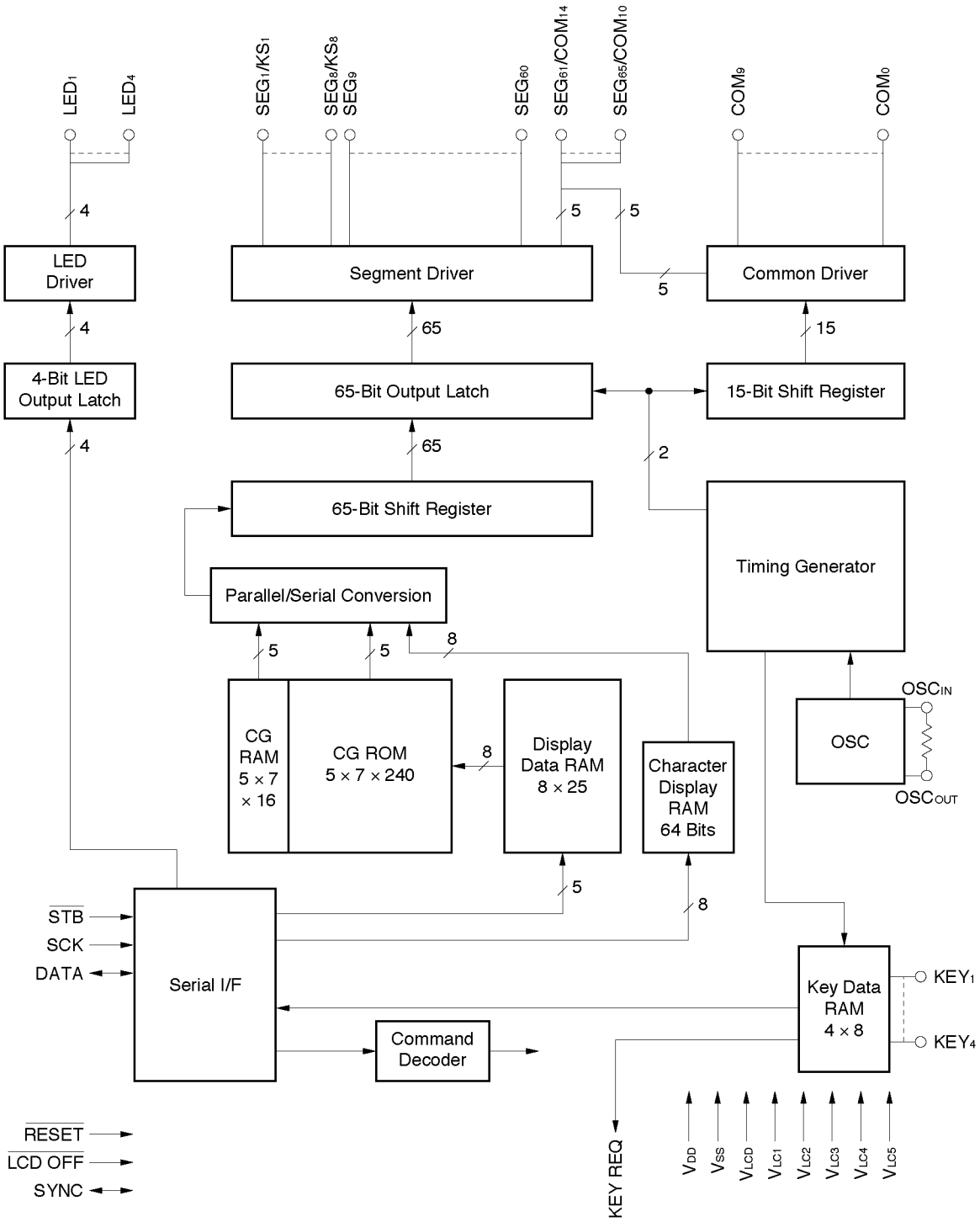
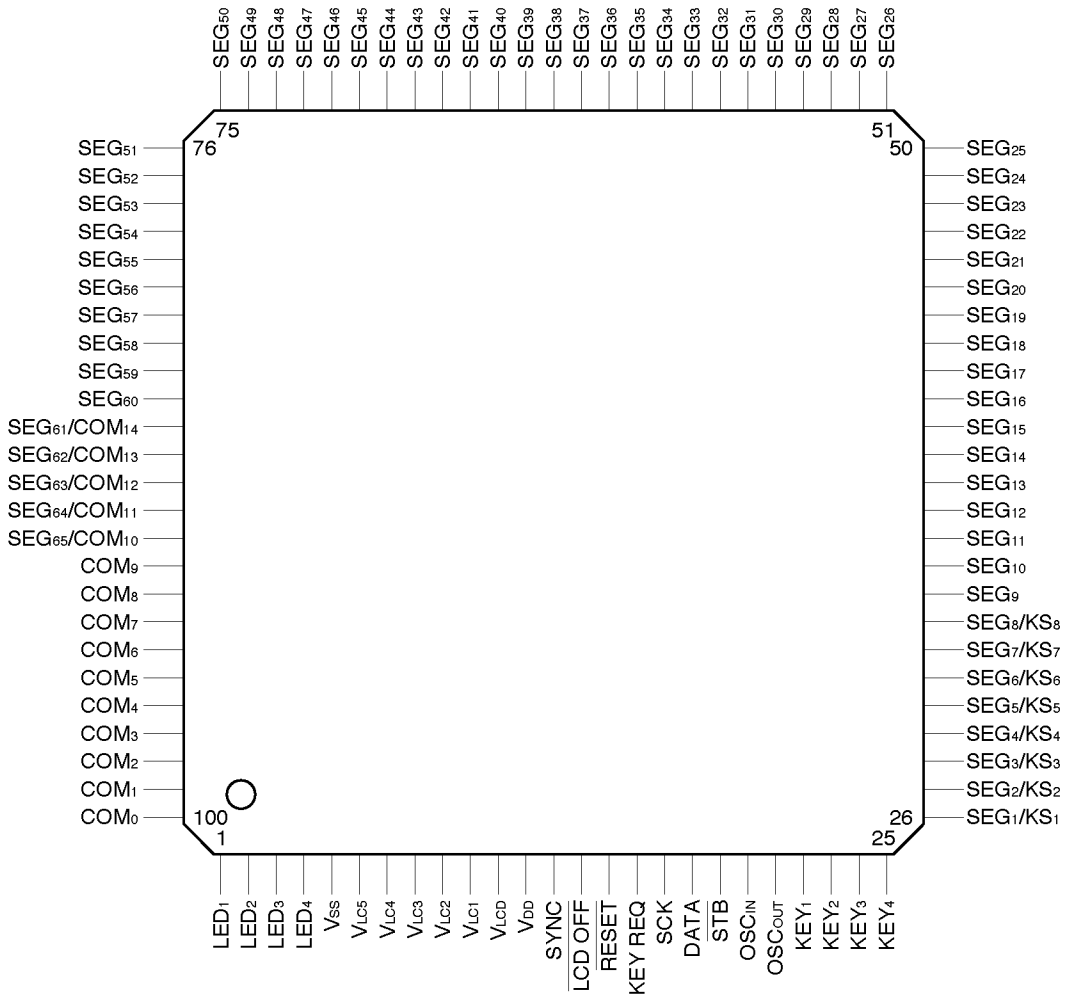
Printed in Japan

BLOCK DIAGRAM



PIN CONFIGURATION



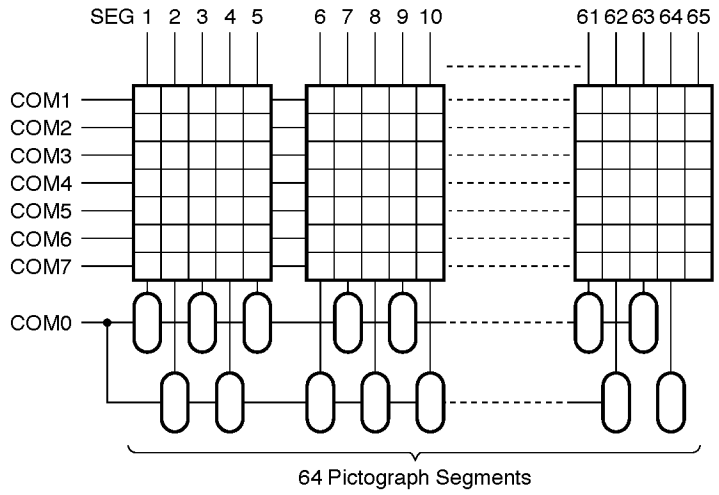
PIN DESCRIPTIONS

Pin Symbol	Pin Name	Pin No.	Function
SEG_1/KS_1 to SEG_8/KS_8	Segment output/key source output dual-function pins	26 to 33	Pins with dual function as dot matrix LCD segment outputs and key scanning key source outputs
SEG_9 to SEG_{60}	Segment outputs	34 to 85	Dot matrix LCD segment outputs
SEG_{61}/COM_{14} to SEG_{85}/COM_{10}	Segment output/common output dual-function pins	86 to 90	Switchable to either dot matrix LCD segment outputs or common outputs
COM_0 to COM_9	Common outputs	91 to 100	Dot matrix LCD common outputs
LED_1 to LED_4	LED output pins	1 to 4	LED outputs are Nch open-drain.
SCK	Shift clock input	17	Data shift clock Data is read on rising edge, and output on falling edge.
DATA	Data input/output	18	Performs input of commands, key data, etc., and key data output. Input is performed from the MSB on the rise of the shift clock, and the first 8 bits are recognized as a command. Output is performed from the MSB on the fall of the shift clock. Output is Nch open-drain.
$\overline{STB}$	Strobe input	19	Data input is enabled when "H". Command processing is performed on a fall.
KEY REQ	Key request output	16	"H" if there is key data, "L" if there is none. Key data can be read irrespective of the state of this pin. Output is CMOS output.
$\overline{RESET}$	Reset input	15	Initial state is set when "L".
$\overline{LCD\ OFF}$	LCD off input	14	When "L", a forced LCD off operation is performed, and SEG_n & COM_n output the unselected waveform.
SYNC	Synchro	13	Synchronization signal input/output pin. When 2 or more chips are used, wired-OR connection is made to each chip. A pull-up resistor is also required when one chip is used.
OSC_{IN}	Oscillation pins	20	Connect oscillator resistor.
OSC_{OUT}		21	
KEY_1 to KEY_4	Key data inputs	22 to 25	Key scanning key data inputs.
V_{DD}	Logic power supply pin	12	Internal logic power supply pin
V_{SS}	GND pin	5	GND pin
V_{LCD}	LCD drive voltage pin	11	LCD drive power supply pin
V_{LC1} to V_{LC5}	LCD drive power supply	10 to 6	Dot matrix LCD drive power supply

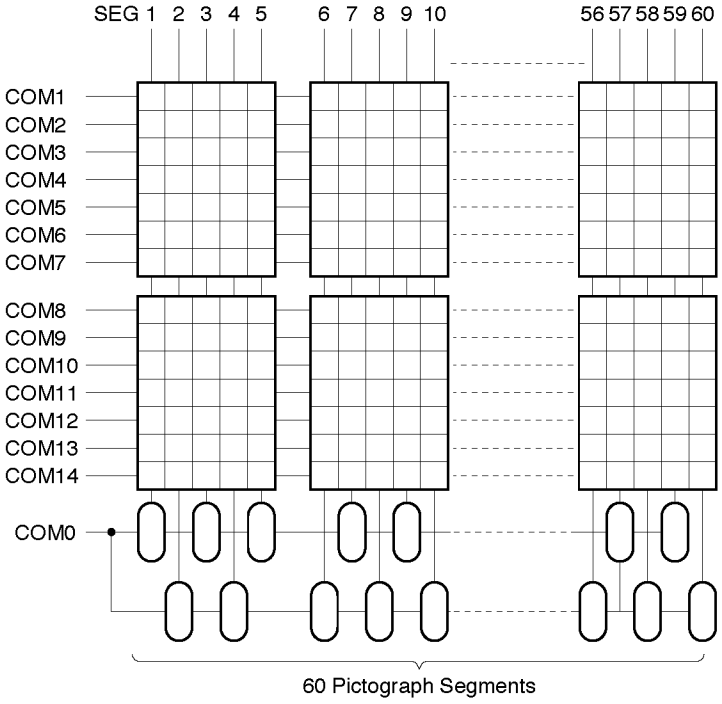
LCD DISPLAY

In the μPD16432B LCD display, a 5 × 7-segment display and pictograph display segments can be driven. The pictograph display segment common output is allocated to COM_0, and up to 64 can be driven.

(1) Example of 1/8 duty connections



(2) Example of 1/15 duty connections



CHARACTER CODES AND CHARACTER PATTERNS

The relation between character codes and character patterns is shown below. Character codes 00H to 0FH are allocated to CGRAM.

Character codes 10H to 1FH and E0H to FFH are undefined.

Higher Bits / Lower Bits	0XH	1XH	2XH	3XH	4XH	5XH	6XH	7XH	8XH	9XH	AXH	BXH	CXH	DXH	EXH	FXH
X0HRAM	CG (1)															
X1HRAM	CG (2)															
X2HRAM	CG (3)															
X3HRAM	CG (4)															
X4HRAM	CG (5)															
X5HRAM	CG (6)															
X6HRAM	CG (7)															
X7HRAM	CG (8)															
X8HRAM	CG (9)															
X9HRAM	CG (10)															
XAHRAM	CG (11)															
XBHRAM	CG (12)															
XCHRAM	CG (13)															
XDHRAM	CG (14)															
XEHRAM	CG (15)															
XFHRAM	CG (16)															

DISPLAY RAM ADDRESSES

Display RAM addresses are allocated as shown below irrespective of the display mode.

Column No.	1	2	3	4	5	6	7	8	9	10	11	12	13
Line 1	00H	01H	02H	03H	04H	05H	06H	07H	08H	09H	0AH	0BH	0CH
Line 2	0DH	0EH	0FH	10H	11H	12H	13H	14H	15H	16H	17H	18H	

PICTOGRAPH DISPLAY RAM ADDRESSES

Pictograph display RAM addresses are allocated as shown below.

Address	Segment Output No.							
	b7	b6	b5	b4	b3	b2	b1	b0
00H	1	2	3	4	5	6	7	8
01H	9	10	11	12	13	14	15	16
02H	17	18	19	20	21	22	23	24
03H	25	26	27	28	29	30	31	32
04H	33	34	35	36	37	38	39	40
05H	41	42	43	44	45	46	47	48
06H	49	50	51	52	53	54	55	56
07H	57	58	59	60	61	62	63	64

Note When 1/15 duty is used (12 columns × 2 lines), 61 to 64 are disabled.

CGRAM COLUMN ADDRESSES

A maximum of any sixteen 5 × 7-dot characters can be written in CGRAM. The row address within one character is allocated as shown below, and is specified by bits b7 to b5.

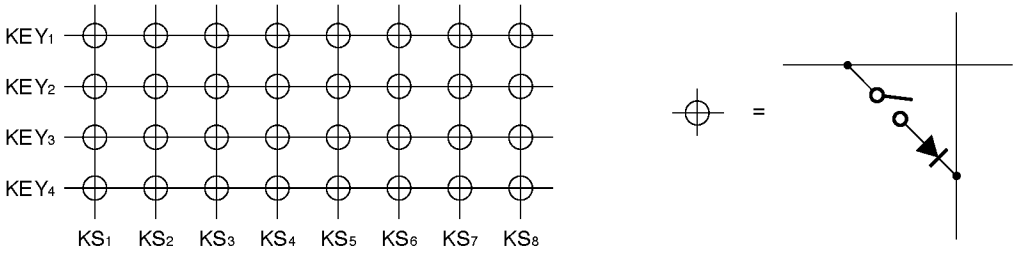
The character code for which a write is to be performed must be specified beforehand with an address setting command.

Row Address	Dot Data							
	b7	b6	b5	b4	b3	b2	b1	b0
00H	0	0	0	*	*	*	*	*
01H	0	0	1	*	*	*	*	*
02H	0	1	0	*	*	*	*	*
03H	0	1	1	*	*	*	*	*
04H	1	0	0	*	*	*	*	*
05H	1	0	1	*	*	*	*	*
06H	1	1	0	*	*	*	*	*
	Row Address			Font Data (5 × 7 Dots)				

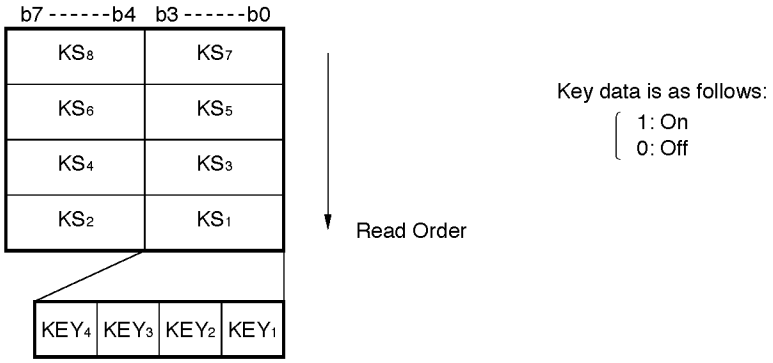
* Font data (1: on, 0: off)

KEY MATRIX AND KEY DATA RAM CONFIGURATION

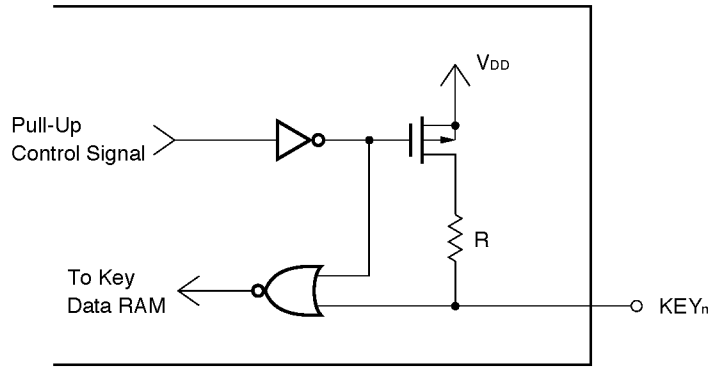
The key matrix has an 8 × 4 configuration, as shown below.



Key data is stored as shown below, and is read in MSB-first order by a read command.



Key Input Equivalent Circuit



- In the event of key source output, the pull-up control signal becomes “H”, and the pull-up transistor is turned on.

KEY REQUEST (KEY REQ)

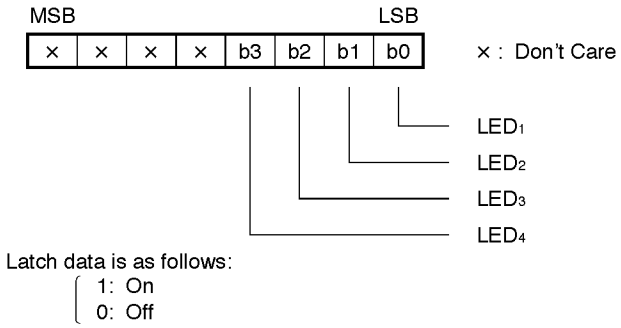
A key request is output as shown below according to the state.

State	KEY REQ[Note]	Key Scan Internal Pull-Up Resistor
In key scan operation	High level is output while any key data is "1".[Note]	During key scan : ON During display : OFF
In standby mode or when SEG_n & COM_n are fixed at V_{LC5}	High level is output in case of key input only.	Always ON
When key scanning is stopped	Fixed at low level	Always OFF

Note KEY REQ does not become low until the key data is all "0".
(It is not synchronized with the key data reads.)

LED OUTPUT LATCH CONFIGURATION

The low-order 4 bits of the LED output latch are enabled, and the high-order 4 bits disabled, as shown below.



COMMANDS

Commands set the display mode and status.

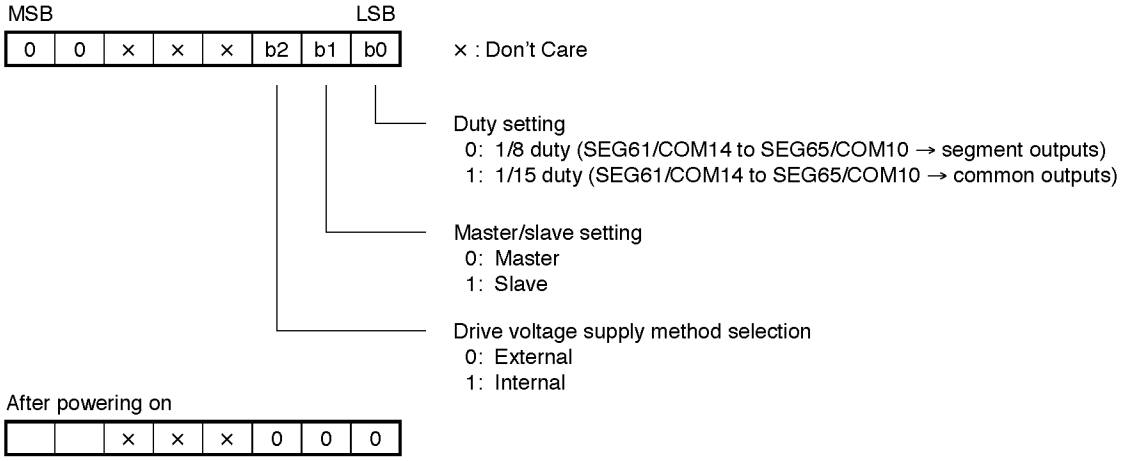
The first byte after a rise edge on the $\overline{STB}$ pin is regarded as a command.

If $\overline{STB}$ is driven low during command/data transfer, serial communication is initialized and the command/data being transferred is invalidated. (However, a command or data that has already been transferred is valid.)

(1) Display Setting Command

This command initializes the μPD16432B[Note], and sets the duty, number of segments, number of commons, master/slave operation, and the drive voltage supply method.

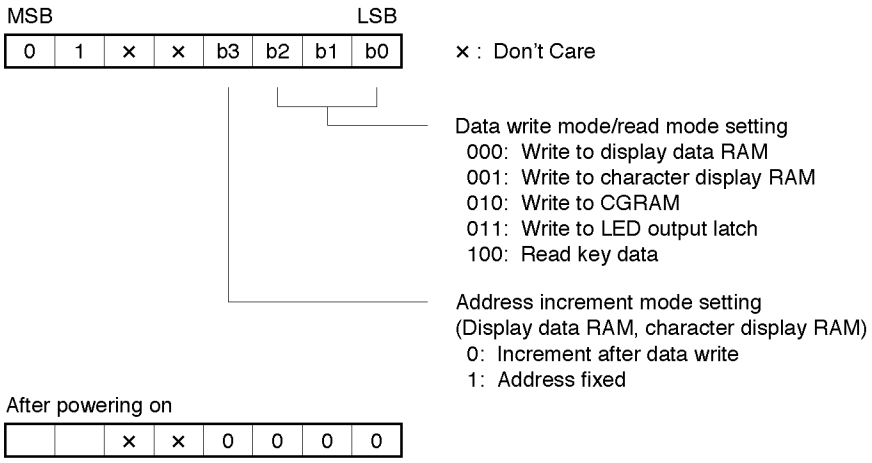
The state set when this command is executed is: LCD off, LED on, key scanning stopped. To restart the display, it is necessary to execute "status command" normal operation. However, nothing is done if the same mode is selected.



Note When multiple chips are used, only the chip that sent the command is enabled. If initialization is performed during display, the display may be affected (especially when multiple chips are used).

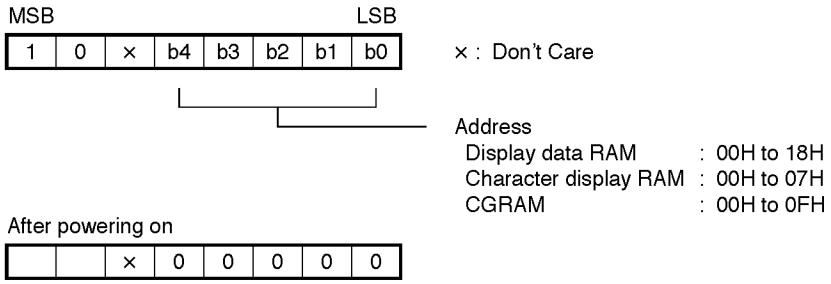
(2) Data Setting Command

Sets the data write mode, read mode, and address increment mode.



(3) Address Setting Command

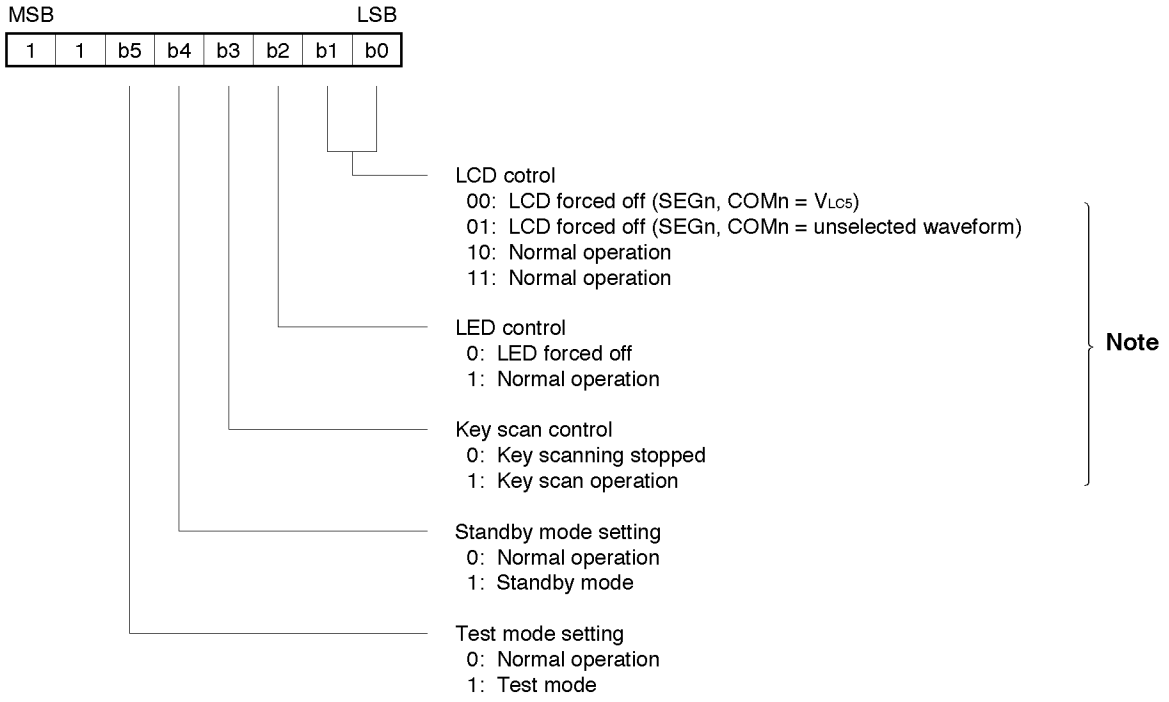
Sets the display data RAM or character display RAM address.



Note If an unspecified address is set, data cannot be written until a correct address is next set. The address is not incremented even in increment mode.

(4) Status Command

Controls the status of the μPD16432.



Note The following states are use prohibited modes, and key scanning does not operate if these states are set.

		0	0	1	0	0	0

		0	0	1	1	0	0

STANDBY MODE

If standby mode is selected with bit b4 of the status command, the following state is set irrespective of bits b3 to b0 of the status command.

(1) LCD forced off (SEG_n, $COM_n = V_{LC5}$)
(2) LED forced off
(3) Key scanning stopped (but KEY_n = key input wait)
(4) OSC stopped

There are two ways of releasing standby mode, as follows:

(1) Using Status Command

Select normal operation with bit b4 of the status command.

Example of Use of Status Command

Item	$\overline{STB}$	Command/Data								Description
		b7	b6	b5	b4	b3	b2	b1	b0	
Standby mode	L									
Status command	H	1	1	0	0	0	0	0	0	Standby release (OSC oscillation start), LCD control off (SEG_n, $COM_n = V_{LC5}$), LED forced off, key scanning stopped
Standby transition time	L									10 μs[Note]
Status command	H	1	1	0	0	1	1	1	0	Normal operation
End	L									

Note If LCD normal operation or key scan operation is initiated within the standby transition time, the LCD may flicker.

(2) Using KEYn

If any key is set to the ON state, the standby mode is released and OSC oscillation starts. Also, KEY REQ is set to "H", informing the microcomputer that a key has been pressed and standby mode has been released. In this state, the key data is not memorized, and therefore it is necessary to set key scanning to the normal state after the standby transition time, and fetch the key data.

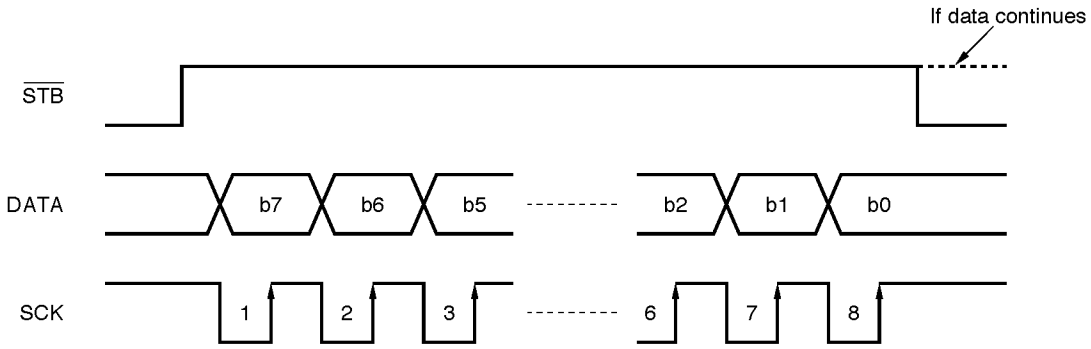
Example of Use of KEYn

Item	$\overline{STB}$	Command/Data								Description
		b7	b6	b5	b4	b3	b2	b1	b0	
Standby mode	L									
Key data present	L									Standby release (KEY REQ = H, OSC oscillation start)
Standby transition time	L									10 μs[Note]
Status command	H	1	1	0	0	1	0	0	1	LCD forced off (unselected waveform), LED forced off, key scan operation
Key scan	L									1 frame or more
Data setting command	H	0	1	0	0	0	1	0	0	Key data read, address increment
Key data	H	*	*	*	*	*	*	*	*	For KS_8, KS_7
Key data	H	*	*	*	*	*	*	*	*	For KS_6, KS_5
Key data	H	*	*	*	*	*	*	*	*	For KS_4, KS_3
Key data	H	*	*	*	*	*	*	*	*	For KS_2, KS_1
End	L									Key distinction

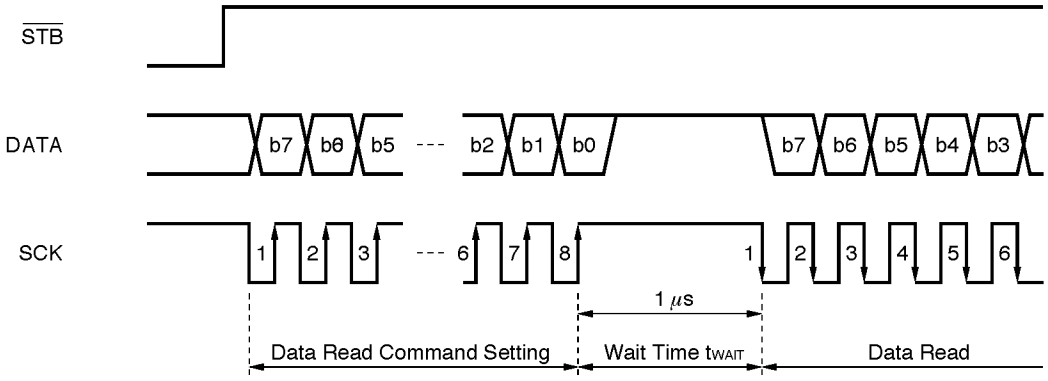
Note If LCD normal operation or key scan operation is initiated within the standby transition time, the LCD may flicker.

SERIAL COMMUNICATION FORMATS

(1) Reception (Command/Data Write)



(2) Transmission (Command/Data Read)



Caution **As the DATA pin is an Nch open-drain output, a pull-up resistor must be connected externally. (1 kΩ to 10 kΩ)**

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C, V_{SS} = 0 V)

Parameter	Symbol	Rating	Unit
Logic supply voltage	V_{DD}	–0.3 to +7.0	V
Logic input voltage	V_{IN}	–0.3 to +V_{DD} + 0.3	V
Logic output voltage (Dout, LED)	V_{OUT}	–0.3 to +7.0	V
LCD drive supply voltage	V_{LCD}	–0.3 to +12.0	V
LCD drive power supply input voltage	V_{LC1} to V_{LC5}	–0.3 to +V_{LCD} + 0.3	V
Driver output voltage (Segment, Common)	V_{OUT2}	–0.3 to +V_{LCD} + 0.3	V
LED drive current	I_{OL1}	20	mA
Package allowable dissipation	P_T	1000	mW
Operating ambient temperature	T_A	–40 to +85	°C
Storage temperature range	T_{stg}	–55 to +150	°C

RECOMMENDED OPERATING RANGES

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Logic supply voltage	V_{DD}	2.7	5.0	5.5	V
LCD drive supply voltage	V_{LCD}	V_{DD}	8.0	10.0	V
Logic input voltage	V_{IN}	0		V_{DD}	V
Driver input voltage	V_{LCD1} to V_{LCD5}	0		V_{LCD}	V
LED drive current	I_{OL1}			15	mA

ELECTRICAL SPECIFICATIONS
(UNLESS SPECIFIED OTHERWISE, T_A = –40 to +85°C, V_{DD} = 5 V ±10%, V_{LCD} = 8 V ±10%)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
High-level input voltage	V_{IH}		0.7 V_{DD}		V_{DD}	V
Low-level input voltage	V_{IL}		0		0.3 V_{DD}	V
High-level input current	I_{IH}	SCK, $\overline{STB}$, $\overline{LCDOFF}$, $\overline{RESET}$, KEY_1 to KEY_4			1	μA
Low-level input current	I_{IL}	SCK, $\overline{STB}$, $\overline{LCDOFF}$, $\overline{RESET}$, KEY_1 to KEY_4			–1	μA
Low-level output voltage	V_{OL1}	LED_1 to LED_4, I_{OL1} = 15 mA			1.0	V
High-level output voltage	V_{OH2}	OSC_{OUT}, KEY REQ, I_{OH2} = –1 mA	0.9 V_{DD}			V
Low-level output voltage	V_{OL2}	DATA, OSC_{OUT}, SYNC, I_{OL2} = 4 mA			0.1 V_{DD}	V
High-level leak current	I_{LOH2}	DATA, SYNC, $V_{IN/OUT}$ = V_{DD}			1	μA
Low-level leak current	I_{LOL2}	DATA, SYNC, $V_{IN/OUT}$ = V_{SS}			–1	μA
Common output ON-resistance	R_{COM}	V_{LCD} to V_{LC5} → COM_0 to COM_{14}, I I_O I = 100 μA			2.4	kΩ
Segment output ON-resistance	R_{SEG}	V_{LCD} to V_{LC5} → SEG_1 to SEG_{60}, I I_O I = 100 μA			4.0	kΩ
Current consumption (Logic)	I_{DD1}	Normal operation[Note], V_I = V_{DD} or V_{SS}, f_{OSC} = 250 kHz			500	μA
	I_{DD2}	Standby mode, V_I = V_{DD} or V_{SS}, f_{OSC} stopped			5	μA
Current consumption (Driver)	I_{LCD1}	Normal operation, internal bias selected, no load			1 000	μA
	I_{LCD2}	Standby mode, internal bias used, no load			5	μA

Note Normal operation: V_{DD} = 5 V, V_{LCD} = 8 V

Remarks TYP. values are reference values for T_A = 25°C.

SWITCHING SPECIFICATIONS

(UNLESS SPECIFIED OTHERWISE, T_A = –40 to +85°C, V_{DD} = V_{LCD} = 5 V ±10%, R_L = 5 kΩ, C_L = 150 pF)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Oscillator frequency	f_{OSC}	R = 100 kΩ	175	250	325	kHz
Output data delay time	t_{PZL}	SCK ↓ → DATA ↓			100	ns
Output data delay time	t_{PLZ}	SCK ↓ → DATA ↑			300	ns
SYNC delay time	t_{DSYNC}				1.5	μs

Note The time for one frame is found as follows.

1 frame = 1/f_{OSC} × 128 clocks × duty number + 1/f_{OSC} × 64 clocks

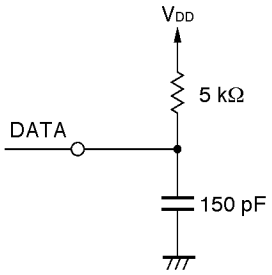
If f_{OSC} = 250 kHz and duty = 1/15, 1 frame = 4 μs × 128 × 15 + 4 μs × 64 = 7.94 ms

REQUIRED TIMING CONDITIONS

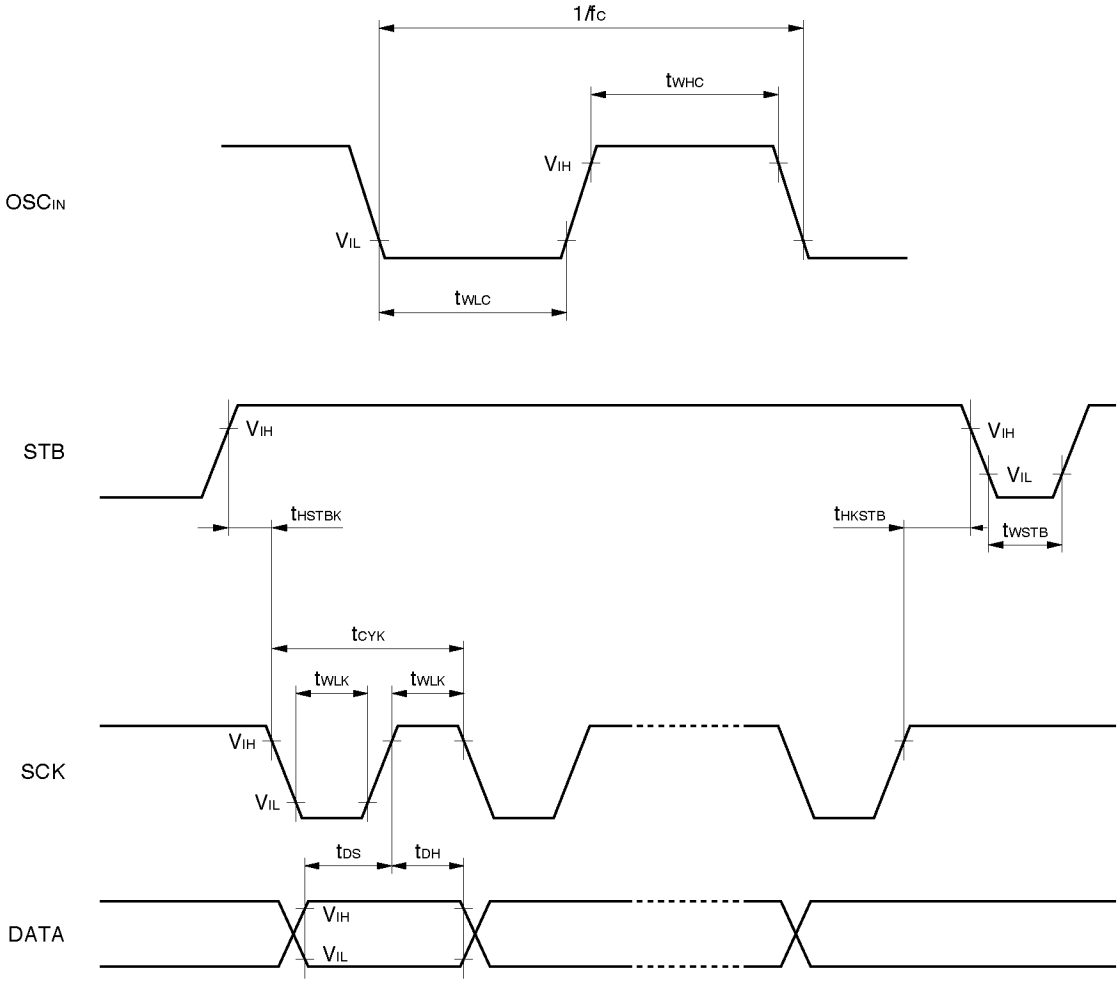
(UNLESS SPECIFIED OTHERWISE, T_A = –40 to +85°C, V_{DD} = 5 V ±10%, V_{LCD} = 8 V ±10%, R_L = 5 kΩ, C_L = 150 pF)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Clock frequency	f_{OSC}	OSC_{IN} external clock	100		500	kHz
High-level clock pulse width	t_{WHC}	OSC_{IN} external clock	1		5	μs
Low-level clock pulse width	t_{WLC}	OSC_{IN} external clock	1		5	μs
Shift-clock cycle	t_{CYK}	SCK	900			ns
High-level shift clock pulse width	t_{WHK}	SCK	400			ns
Low-level shift clock pulse width	t_{WLK}	SCK	400			ns
Shift clock hold time	t_{HSTBK}	STB ↑ → SCK ↓	1.5			μs
Data setup time	t_{DS}	DATA → SCK ↑	100			ns
Data hold time	t_{DH}	SCK ↑ → DATA	200			ns
STB hold time	t_{HKSTB}	SCK ↑ → STB ↓	1			μs
STB hold time	t_{WSTB}		1			μs
Wait time	t_{WAIT}	8th SCK ↑ → 9th SCK ↓, in data read	1			μs
SYNC removal time	t_{SREM}		250			ns
Standby transition time	t_{PSTB}		10			μs
Reset pulse width	t_{WRS}	RESET	0.1			μs
Power-ON reset time	t_{PON}	From Power-ON	4			CLK

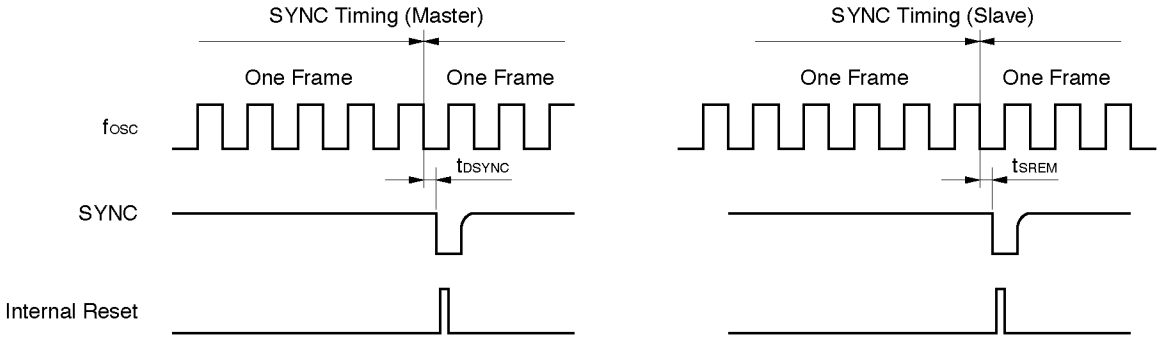
OUTPUT LOAD CIRCUIT

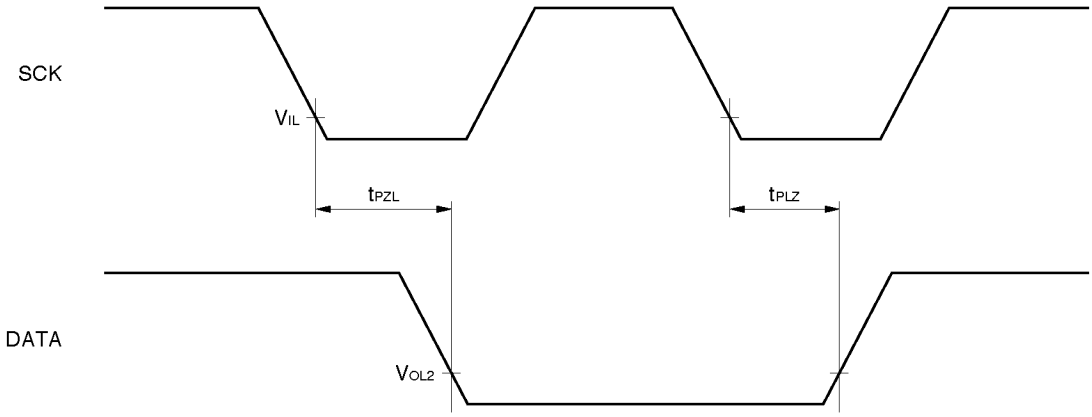


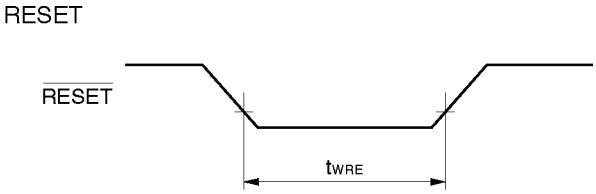
SWITCHING SPECIFICATION WAVEFORM DIAGRAMS



SWITCHING SPECIFICATION WAVEFORM DIAGRAMS

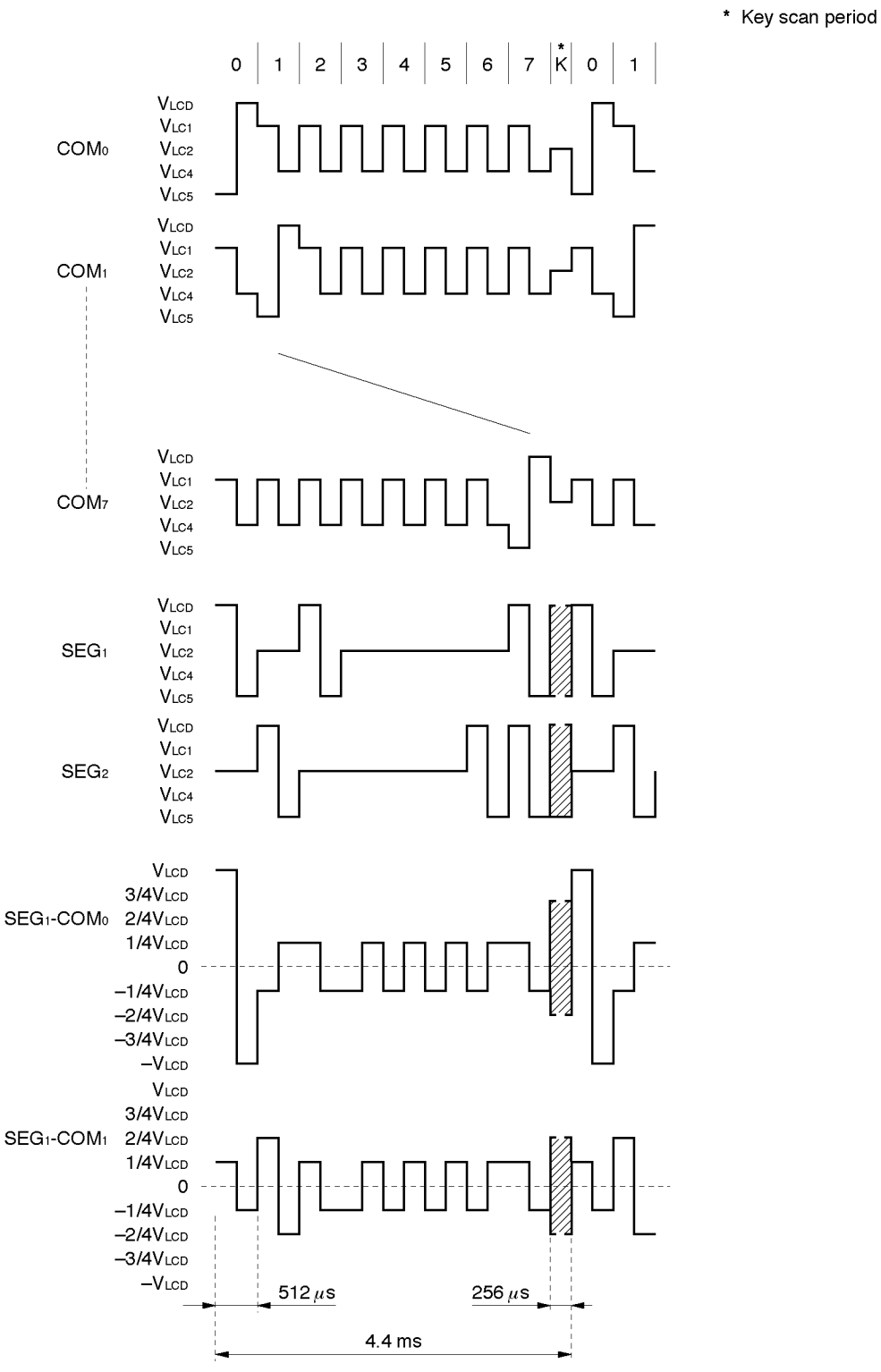




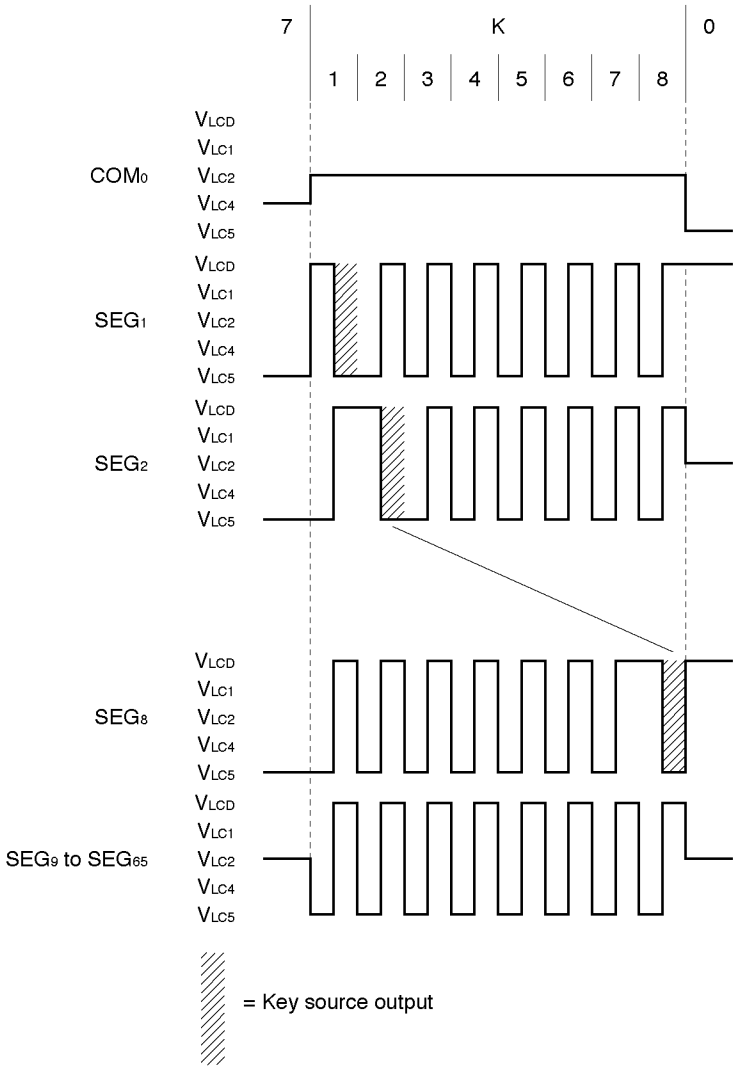


OUTPUT WAVEFORMS

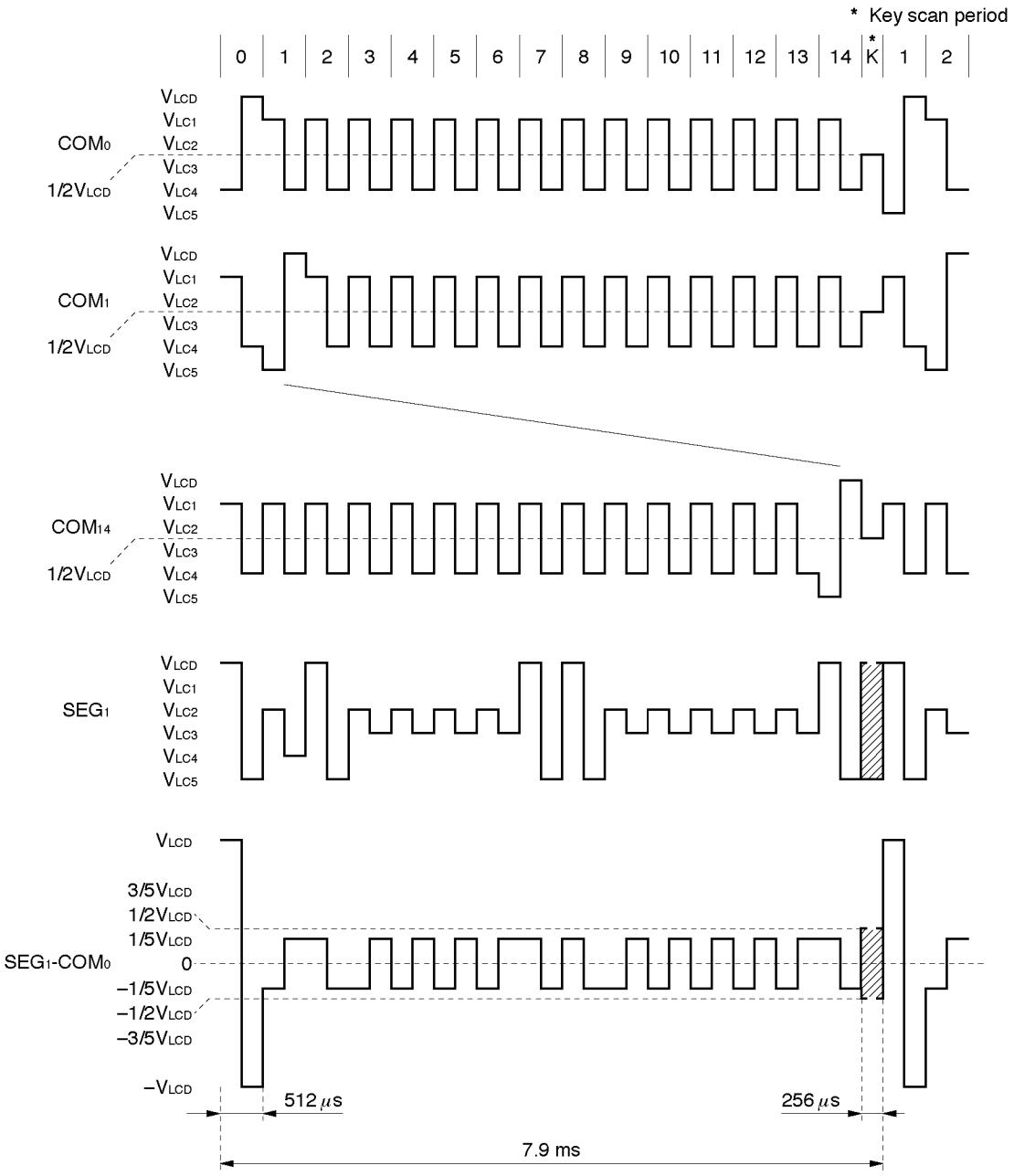
(1) 1/8 Duty (1/4 Bias: VLC2: VLC3)



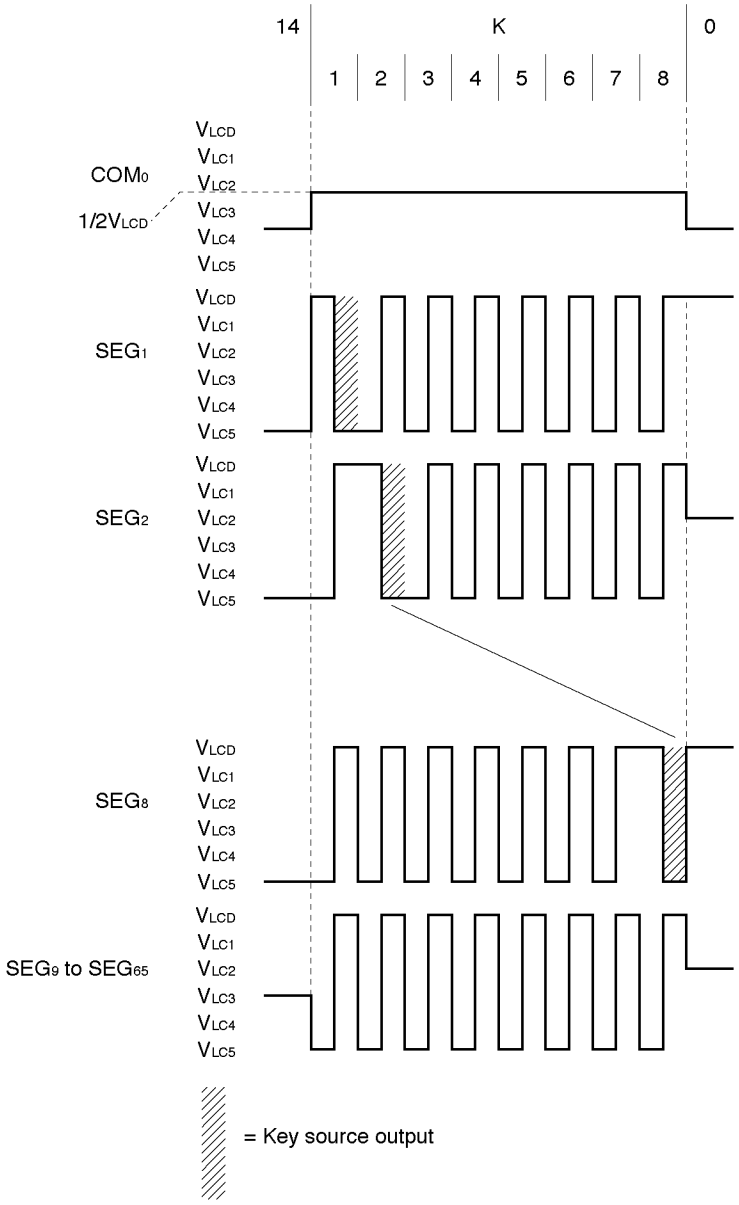
Enlargement of Key Scan Period



(2) 1/15 Duty (1/5 Bias)



Enlargement of Key Scan Period

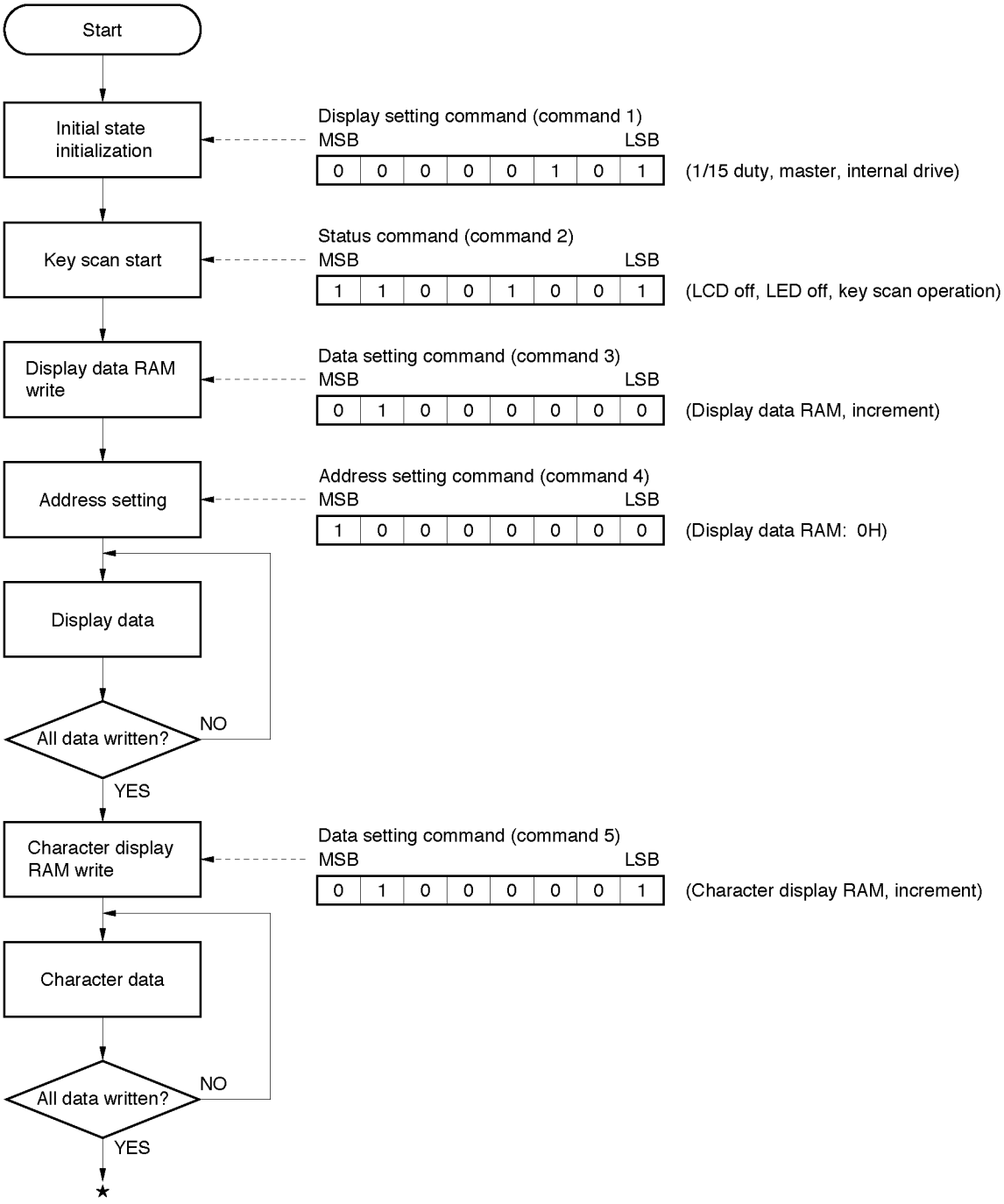


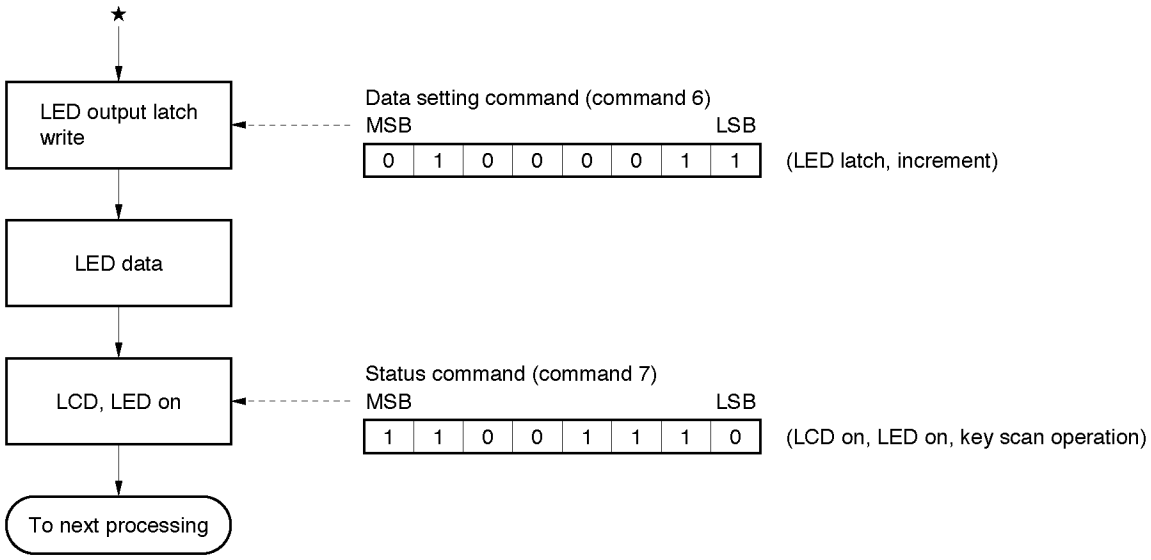
ACCESS PROCEDURES

Access procedures are illustrated below by means of flowcharts and timing charts.

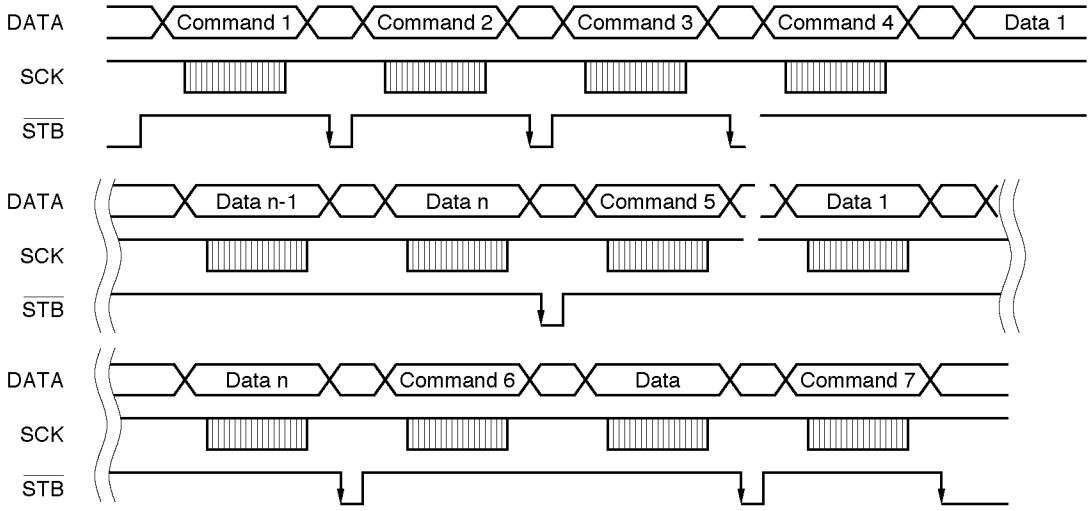
1. Initialization

(1) Flowchart



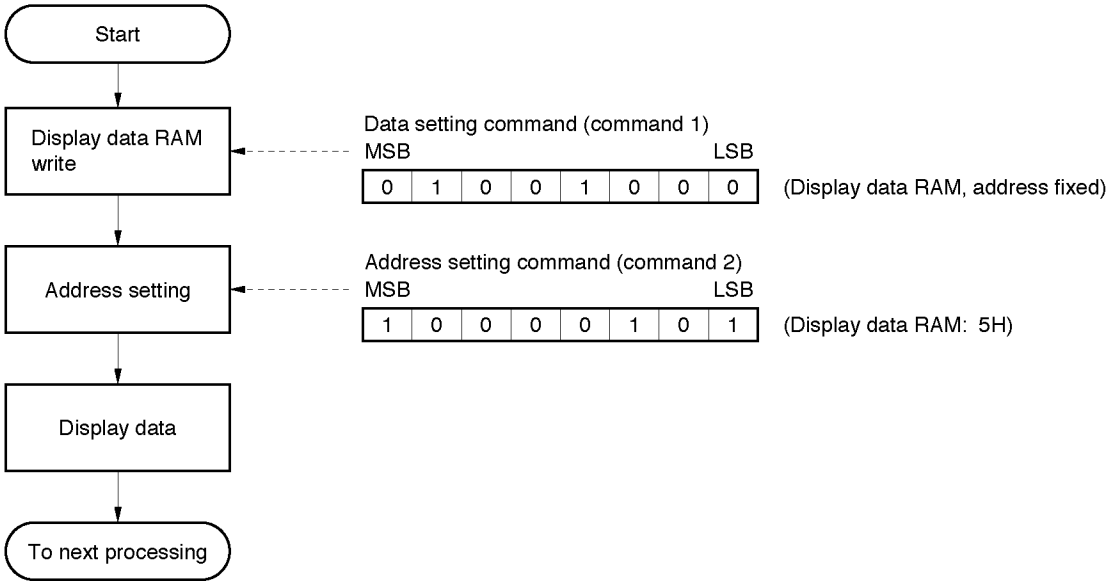


(2) Timing chart

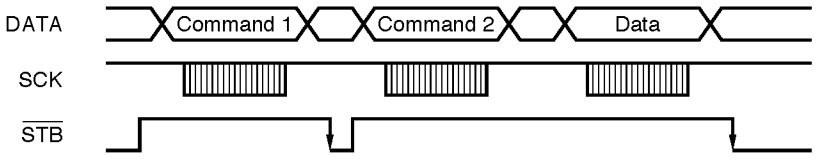


2. Display Data Rewrite (Address Setting)

(1) Flowchart

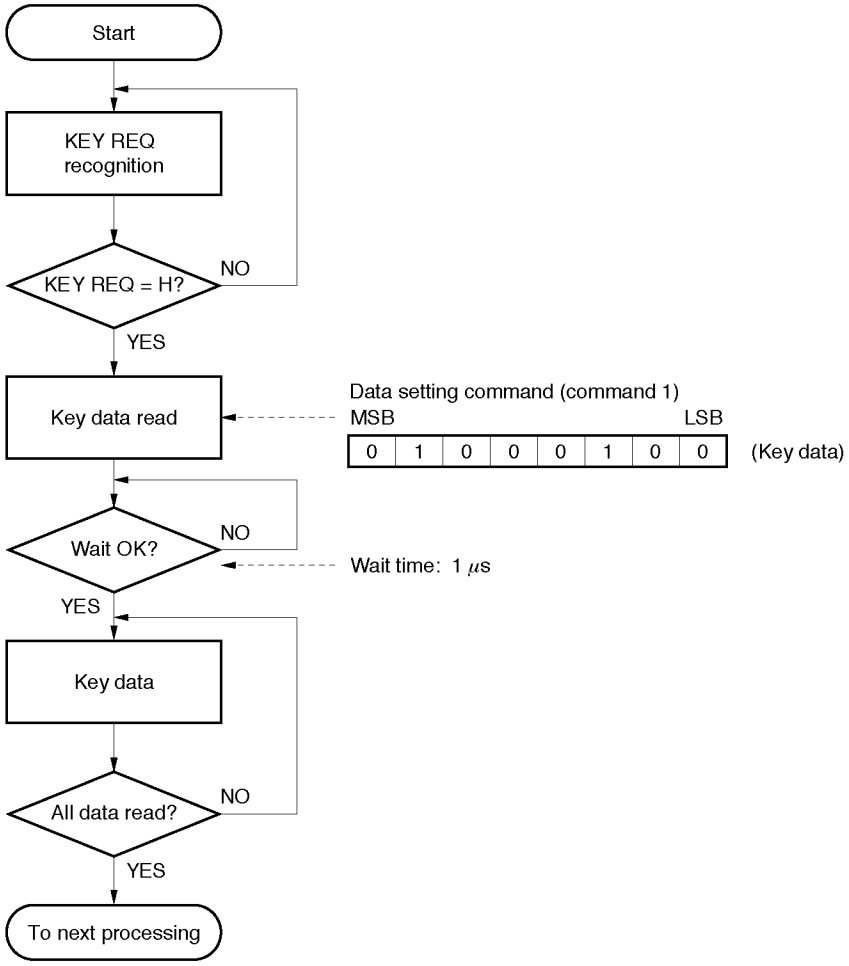


(2) Timing chart

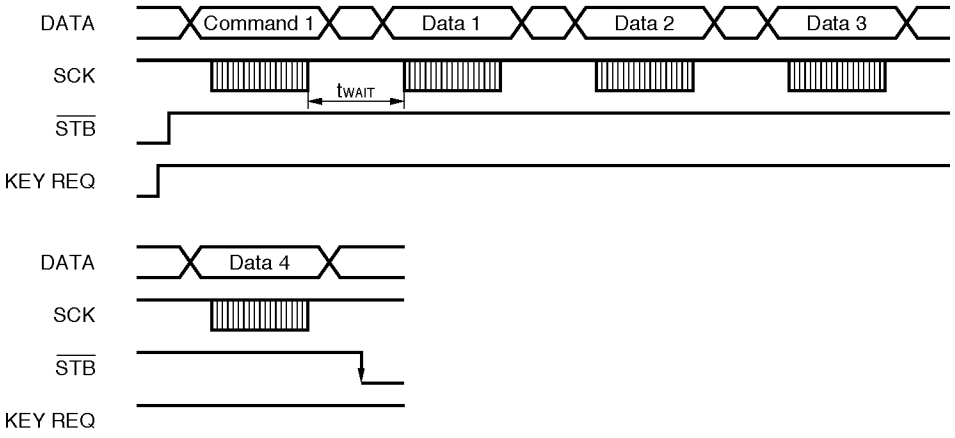


3. Key Data Read

(1) Flowchart



(2) Timing chart

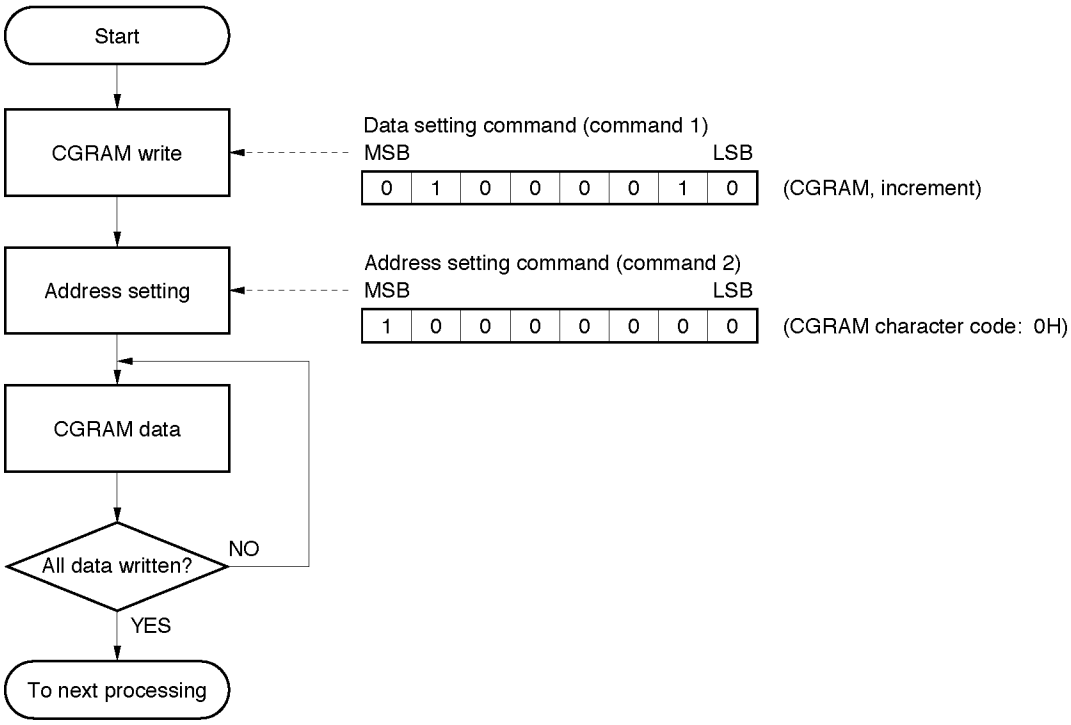


Cautions 1. Wait time t_{WAIT} (1 μs) is necessary from the rise of the 8th shift clock of command 1 until the fall of the 1st shift clock of data 1.

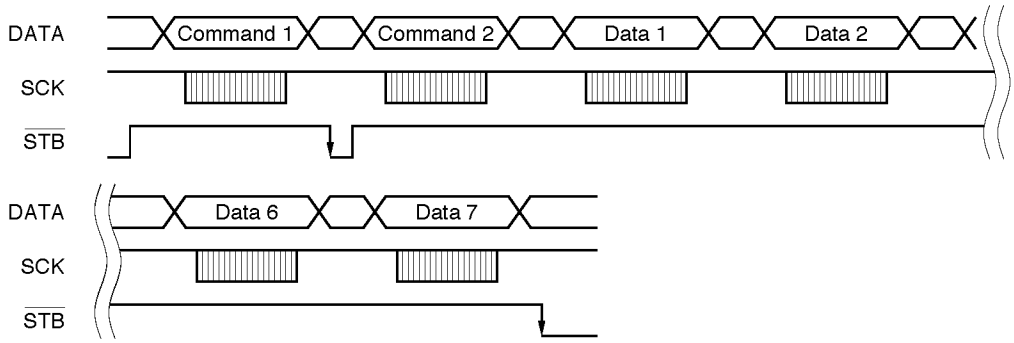
2. KEY REQ does not become low until the key data is all "0".
(It is not synchronized with the key data reads.)

4. CGRAM Write

(1) Flowchart

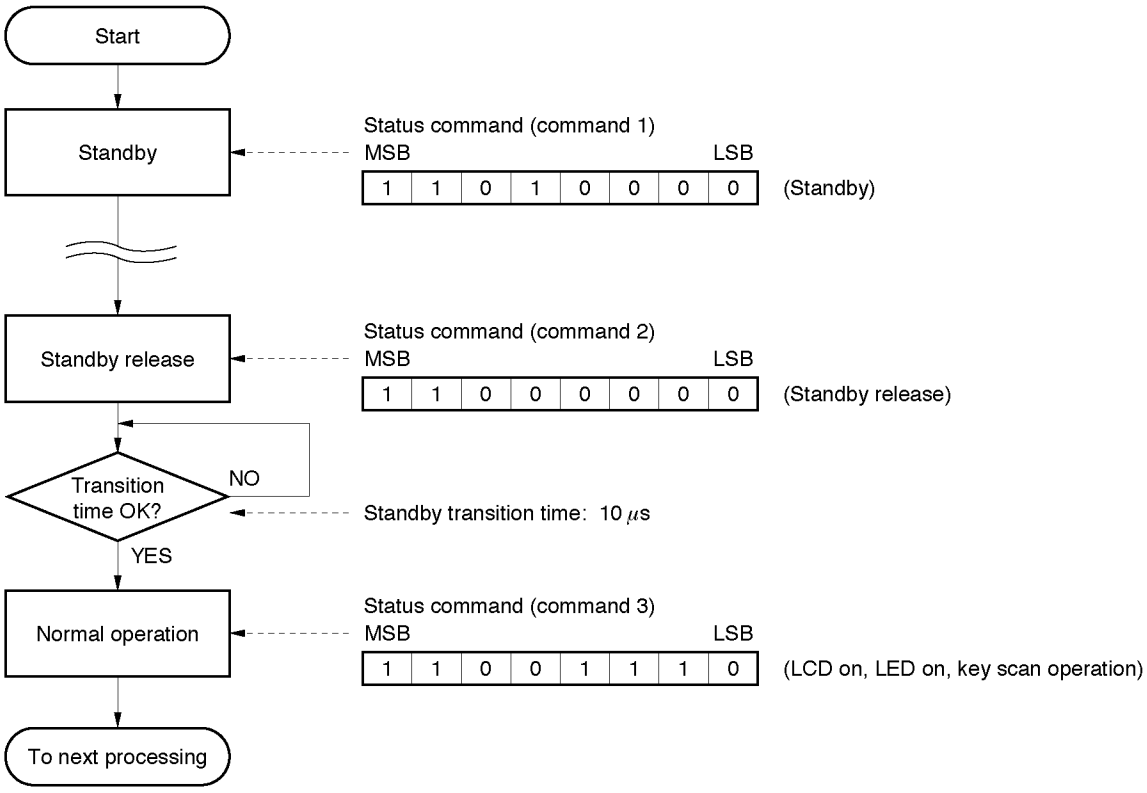


(2) Timing chart

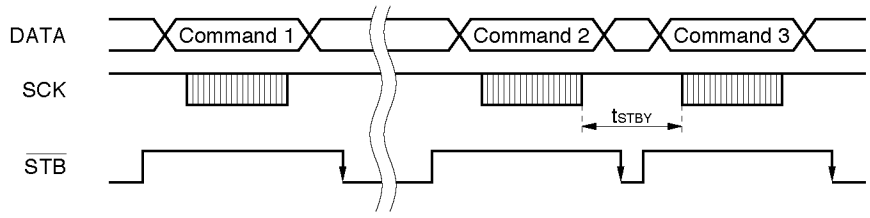


5. Standby (Released by Status Command)

(1) Flowchart

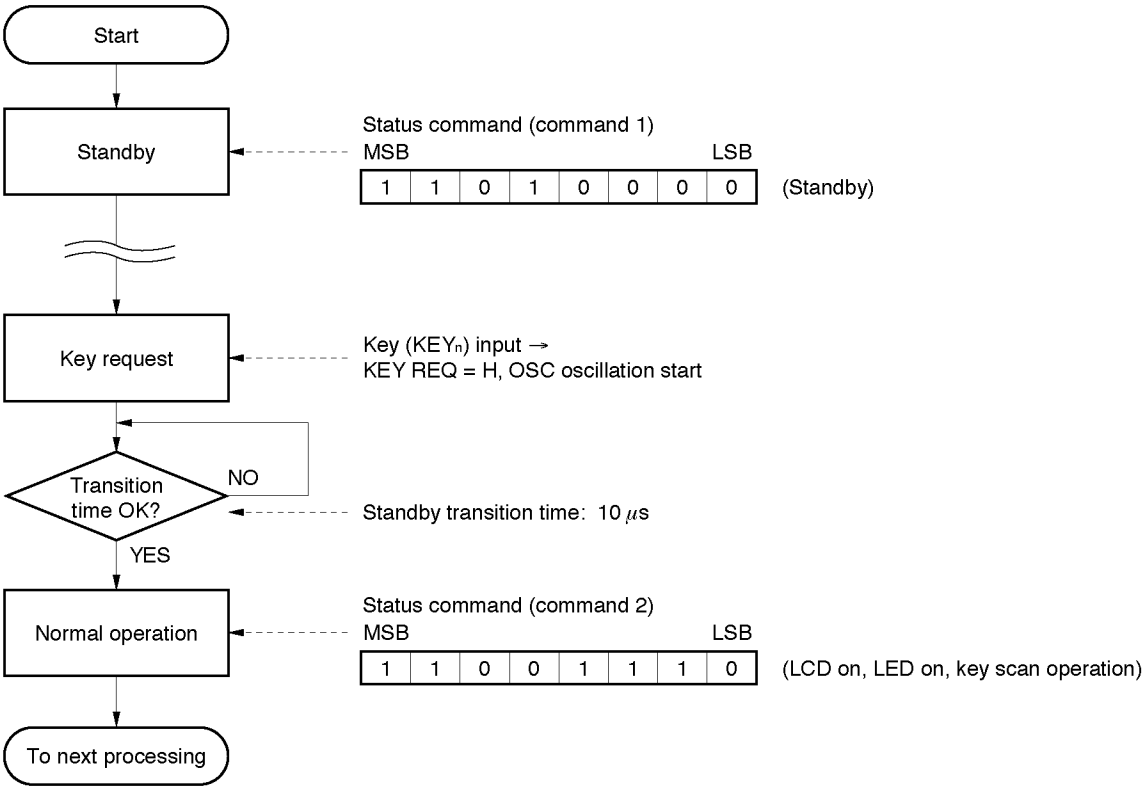


(2) Timing chart

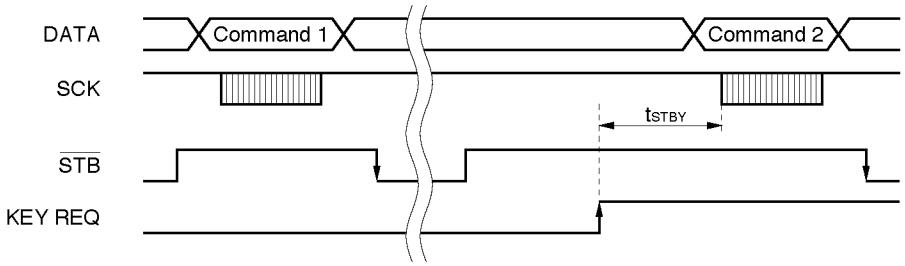


6. Standby (Released by KEYN)

(1) Flowchart

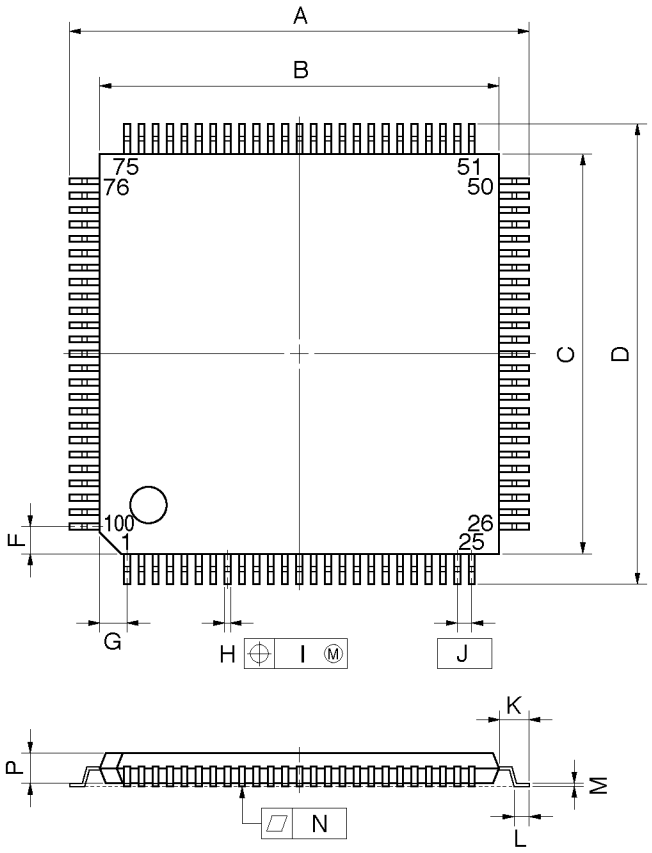


(2) Timing chart

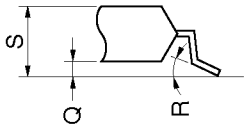


PACKAGE INFORMATION (UNIT: mm)

100 PIN PLASTIC TQFP (FINE PITCH) (□14)



detail of lead end



NOTE

Each lead centerline is located within 0.10 mm (0.004 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	16.0±0.2	0.630±0.008
B	14.0±0.2	$0.551^{+0.009}_{-0.008}$
C	14.0±0.2	$0.551^{+0.009}_{-0.008}$
D	16.0±0.2	0.630±0.008
F	1.0	0.039
G	1.0	0.039
H	$0.22^{+0.05}_{-0.04}$	0.009±0.002
I	0.10	0.004
J	0.5 (T.P.)	0.020 (T.P.)
K	1.0±0.2	$0.039^{+0.009}_{-0.008}$
L	0.5±0.2	$0.020^{+0.008}_{-0.009}$
M	$0.145^{+0.055}_{-0.045}$	0.006±0.002
N	0.10	0.004
P	1.0±0.1	$0.039^{+0.005}_{-0.004}$
Q	0.1±0.05	0.004±0.002
R	$3°^{+7°}_{-3°}$	$3°^{+7°}_{-3°}$
S	1.27 MAX.	0.050 MAX.

S100GC-50-9EU-1

REFERENCE DOCUMENTS

NEC Semiconductor Device Reliability/Quality Control System	(IEI-1212)
Semiconductor Device Mounting Technology Manual	(C10535E)

[MEMO]

M4 96.5