Versatile Interface Adapter Differences

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INTRODUCTION

The Versatile Interface Adapter (VIA) is a very flexible I/O control device. This device contains two 8-bit bidirectional ports, two 16-bit interval timers and a serial-to-parallel/parallel-to-serial shift register. In addition, input data latching and expanded handshaking capability on the I/O ports allow positive control of bidirectional data transfers between the host processor and peripheral devices.

SUMMARY

Three versions of the VIA are available to accommodate the bus interface requirements of both synchronous and asynchronous host systems. The NMOS R6522 is compatible with the 6500 and 6800 families. The CMOS R65C22 can interface to 68000 and 68010 systems. Finally, the CMOS R65NC22 is compatible with 6500, 6800, 68000, 68010, and 68020 microprocessors. All versions are pin compatible. Table 1 summarizes the differences among the three versions of the VIA.

Table 1. R6522, R65C22 and R65NC22 Differences

	R6522	R65C22	R65NC22
Package Options	40-Pin Ceramic DIP 40-Pin Plastic DIP	40-Pin Ceramic DIP 40-Pin Plastic DIP 44-Pin Plastic PLCC	40-Pin Ceramic DIP 40-Pin Plastic DIP 44-Pin Plastic PLCC
$\phi2$ Clock Options (MHz)	1, 2	1, 2, 3, 4	1, 2, 3, 4
Maximum Power (mW)	700	40 (@4 MHz)	40 (@4 MHz)
Host System Compatibility	6500, 6800	6500, 6800, 68000, 68010	6500, 6800, 68000, 68010, 68020
RS0-RS1 Decoding	Decoded during $\phi2$.	Decoded during $\phi2$.	Decoded during $\phi2$ if $\overline{CS2}$ is low.
PA0-PA7, CA2 Characteristics	These ports represent one standard TTL load in the input mode and will drive one standard TTL load in output mode.	These ports represent two standard TTL loads in the input mode and will drive two standard TTL loads in the output mode.	These ports represent two standard TTL loads in the input mode and will drive two standard TTL loads in the output mode.
PB0-PB7, CB2 Characteristics	These ports represent one standard TTL load in the input mode and will drive one standard TTL load in the output mode. They have passive pull ups ($\approx3k\Omega$). They can source 1.0 mA at 1.5 Vdc to directly drive Darlington transistor circuits.	These ports represent two standard TTL loads in the input mode and will drive two standard TTL loads in the output mode. They have active pull-ups. They can source 3.2 mA at 1.5 Vdc to directly drive Darlington transistor circuits.	These ports represent one standard TTL load in the input mode and will drive one standard TTL load in the output mode. They have passive pull ups ($\approx3k\Omega$). PB0-PB7 can source 3.2 mA at 1.5 Vdc to directly drive Darlington transistor circuits.
CB1 Characteristics	This pin represents one standard TTL load in the input mode and will drive one standard TTL load in the output mode. It has a passive pull up ($\approx3k\Omega$). It must not change during the last 100 ns of $\phi2$. It must have a pulse width greater than one $\phi2$ clock period.	This pin represents two standard TTL loads in the input mode and will drive two standard TTL loads in the output mode. It can source 3.2 mA at 1.5 Vdc to directly drive Darlington transistor circuits. It has an active pull-up. CB1 must not change during the last 100 ns of $\phi2$. It must have a pulse width greater than one $\phi2$ clock period.	This pin represents one standard TTL load in the input mode and will drive one standard TTL load in the output mode. It has a passive pull up ($\approx3k\Omega$). CB1 can change anytime but is sampled only during $\phi2$. It must have a pulse width greater than one $\phi2$ clock period.